PRODUCTION SPECIFICATION
OF TFT LCD MODULE

Model No. : M238HCT02 B1F

OC PN: PN238CT02-14

CUSTOMER	
CONFIRMED BY	
APPROVED BY	

PREPARED BY	
CONFIRMED BY	

Date	Rev.	Page	Old Description	New Description	Remark
2023.03.15	1.0	All	The specification was first issued		

1. GENERAL DESCRIPTION

1.1 OVERVIEW

The specification is applied to 23.8" **FRAME LESS** module (M238HCT02 B1F) used HKC PN238CT02-14 opencell. This TFT Liquid Crystal Display open cell supports 1920 x 1080 FHD mode with 16.7M (8bit)colors. This product is with driver ICs and a 30-pins-2ch-LVDS circuit board and built in backlight unit.

1.2 General Specifications

Item	Specification	Unit	Note
Active Area	527.04(H)x296.46(V)	mm	
Module Size	**535.00(H) x 313.00(V)*12.20(D)**	mm	
Weight	2.4	kg	Max.
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	1920 * 1080	pixel	
Pixel Pitch (Sub Pixel)	0.2745*0.2745	mm	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.78 M	color	8bit
Display Mode	Normally Black		
Module Brightness	250	Cd/㎡	
Color Chroma	R = (0.651, 0.333)		Typical value measured at DL BLU
	G = (0.319, 0.599)		
	B = (0.148, 0.054)		
	W = (0.310, 0.330)		
Contrast Ratio	3000:1(Typ.)		
View Angle (CR 10)	+89/-89 (H), +89/-89 (V) (Typ.)		
Surface Treatment	Anti-glare, Haze 2.5%, Hard Coating (3H)		

1.3 Mechanical Specification

Item		Min	Typ	Max	Unit	Note
Weight		-100	2400	+100	g	-
Module Size	Horizontal(H)		535.00		mm	1
	Vertical (V)	(TYP)-0.5	313.00	(TYP)+0.5	mm	
	Depth(D)		12.20		mm	

2. Absolute Maximum Ratings

2.1 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[oC]	Note 3
Glass surface temperature (operation)	TGS	0	+65	[oC]	Note 3, Note 4
Operation Humidity	HOP	5	90	[%RH]	
Storage Temperature	TST	-20	+60	[oC]	
Storage Humidity	HST	5	90	[%RH]	Note 3

Note 1: With in Ta (25C)

Note 2: Permanent damage to the device may occur if exceeding maximum values.

Note 3: Temperature and relative humidity range are shown as the below figure.

     1. 90% RH Max

     2. Max wet-bulb temperature at 39

Note 4: Function Judged only
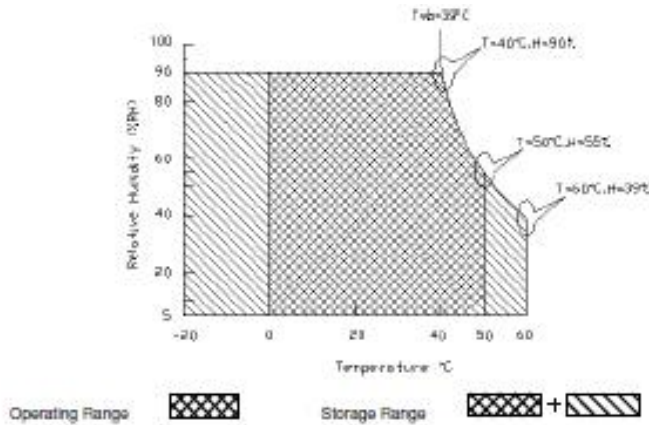
2.2 Backlight Unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LED operation Voltage	V_{led}	56	-	64	V_{led}	
LED operation Current	I_{led}	-	240	-	mA	- / (1)
BackLight Power	P_{BL}	13.44	-	15.36	W	
Lift time	Lt	30000	40000	-	Hrs	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal operating Conditions.

3. ELECTRICAL SPECIFICATIONS

3.1 ELECTRICAL CHARACTERISTICS

3.1.1 Open Cell Power Consumption (TA = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	4.5	5.0	5.5	V	
Ripple Voltage		V_{RP}		-	300	mV	
Power Supply Current	White			0.58	0.65	A	(3.1)
	Color bar H			0.7	0.78	A	(3.2)
	Vertical			0.95	1.1	A	(3.3)
Power Consumption		PLCD		3.5	5.5	Watt	(4)
Rush Current		I_{RUSH}			3	A	(2)
LVDS Interface	Differential Input Voltage	V_{ID}	100		600	mV	(5)
	Common Input Voltage	V_{CM}	$V_{ID}/2$		$2.4 - V_{ID}/2$	V	
	Differential Input High Threshold Voltage	V_{TH}			0.1	V	
	Differential Input Low Threshold Voltage	V_{TL}	-0.1			V	

Note (1) Measurement Conditions

Item	Symbol	Value	Unit
Temperature	A	25±2	℃
Humidity	A	50±10	%RH

Note (2) Vcc rising time=470us
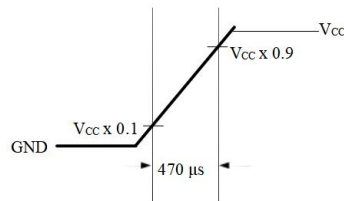
Fig. 3.1 VCC rising time condition

Note (3) Test patterns
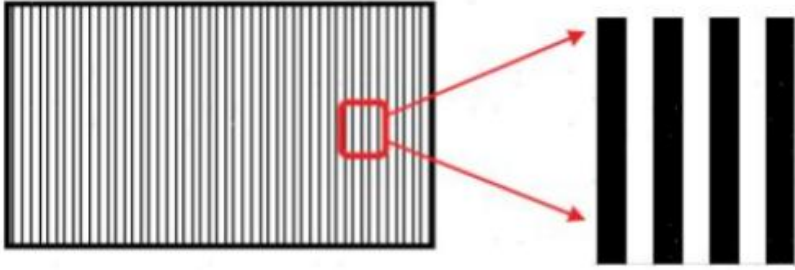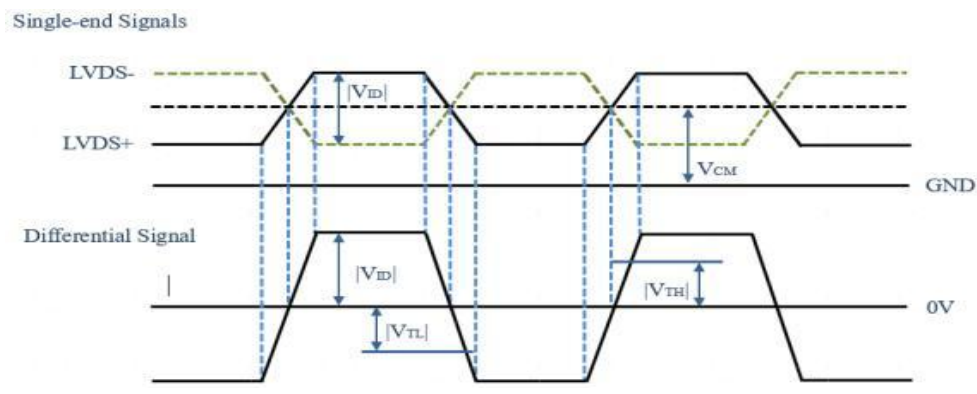A. White Pattern
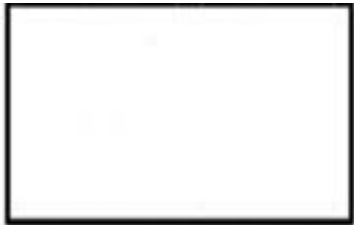
B. color bar H
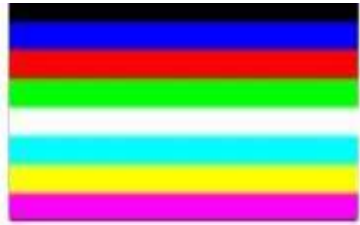
C: Vertical Stripe Pattern

Note (4) The typical power consumption is specified at the pattern with the color bar H, refresh rate is 60Hz, VIN is 5V.

The max power consumption is specified at the pattern with the Horizontal 1 line , refresh rate is 75Hz, VIN is 5V.

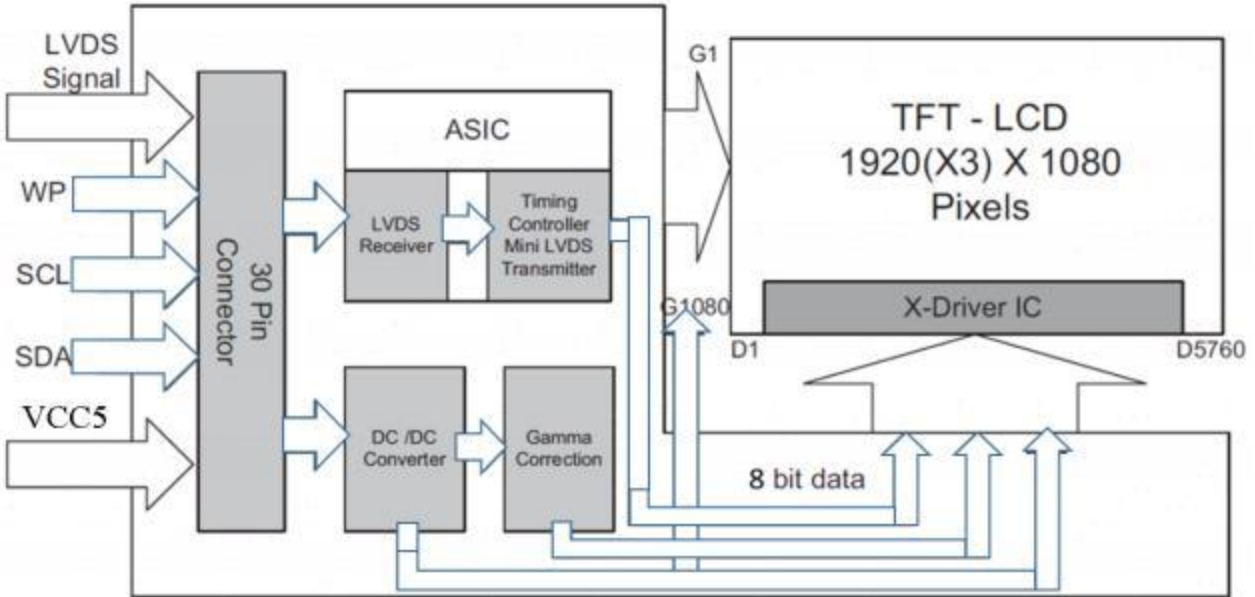Note (5) The LVDS input characteristics are as follows:
Differential Signal

Single-end Signals

LVDS-

$|V_{ID}|$

LVDS+

V_{CM}

GND

Differential Signal

$|V_{ID}|$

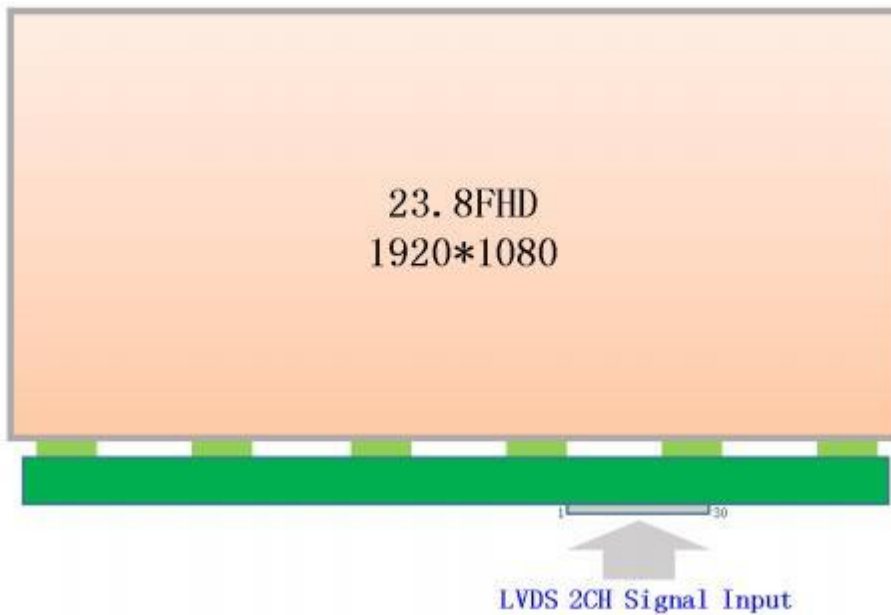$|V_{TH}|$

0V

$|V_{TL}|$

3.2 Block Diagram

The following shows the block diagram of the 23.8 inch Color TFT-LCD Module.

3.3 Block Diagram

3.3.1 Block Diagram of Interface

3.3.2 Interface Pin Assignment For LVDS

CNN: TBD or equivalent

Pin No.	Symbol	Description	Note
1	RXO0-	LVDS Odd Data (-)	
2	RXO0+	LVDS Odd Data (+)	
3	RXO1-	LVDS Odd Data (-)	
4	RXO1+	LVDS Odd Data (+)	
5	RXO2-	LVDS Odd Data (-)	
6	RXO2+	LVDS Odd Data (+)	
7	GND	Power Ground	
8	RXOCLK-	LVDS Odd Clock (-)	
9	RXOCLK+	LVDS Odd Clock (+)	
10	RXO3-	LVDS Odd Data (-)	
11	RXO3+	LVDS Odd Data (+)	
12	RXE0-	LVDS Even Data (-)	
13	RXE0+	LVDS Even Data (+)	
14	GND	Power Ground	
15	RXE1-	LVDS Even Data (-)	
16	RXE1+	LVDS Even Data (+)	
17	GND	Power Ground	
18	RXE2-	LVDS Even Data (-)	
19	RXE2+	LVDS Even Data (+)	
20	RXECLK-	LVDS Even Clock (-)	
21	RXECLK+	LVDS Even Clock (+)	
22	RXE3-	LVDS Even Data (-)	
23	RXE3+	LVDS Even Data (+)	
24	WP	Write Protection	
25	SCL	I2C Clock	
26	SDA	I2C Data	
27	BIST_MODE	For HKC test only,no connection	
28	cc	Power supply +5.0V	
29	cc	Power supply +5.0V	
30	cc	Power supply +5.0V	

Interface Connector Information

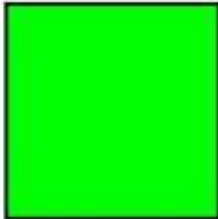| Item	Description
Manufacturer	XDYT
Connector model	SMT 3- 10522317-0

CNN: XDYT or equivalent
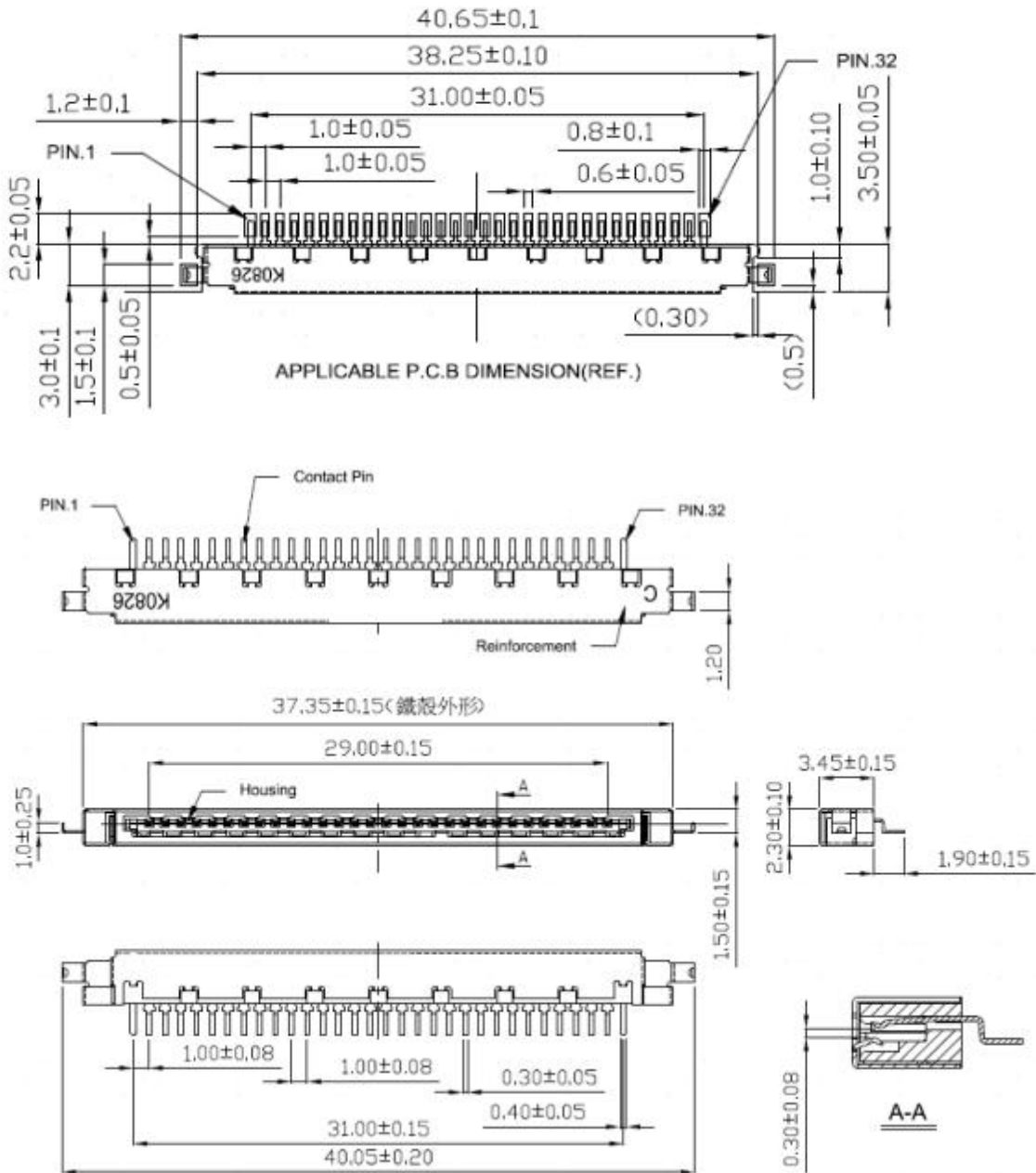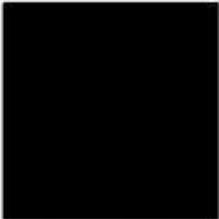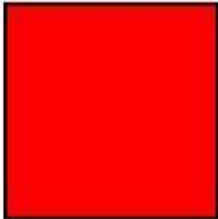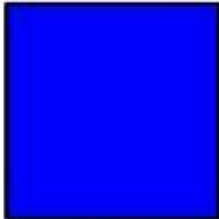
3.3.3 Built-in Self Test Patterns
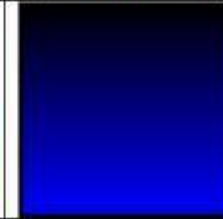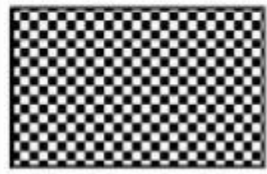
The TCON is built in variable test patterns. The sequence and display time of test patterns could be set

by EEPROM code. An example BIST pattern is as the following table.

PT1: White	PT2: Black	PT3: Full Red	PT4: Full Green	PT5: Full Blue

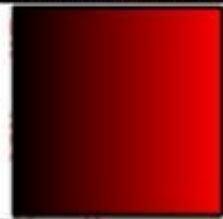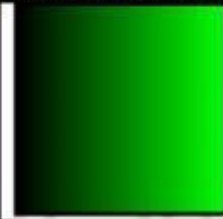| PT6: Full Gray pattern (color gating & Gray level)	PT7: White H Gray (inverse & 64 mode)	PT8: Red H Gray (inverse & 64 mode)	PT9: Green H Gray (inverse & 64 mode)	PTA: Blue H Gray (inverse & 64 mode)

PTB: White V Gray (inverse & 64 mode)	PTC: Red V Gray (inverse & 64 mode)	PTD: Green V Gray (inverse & 64 mode)	PTE: Blue V Gray (inverse & 64 mode)	PTF: Checkboard (inverse)

PT10: V Grayscale 16level	PT11: V Grayscale 32level	PT12: V Grayscale 64level	PT13: H Grayscale 16level	PT14: H Grayscale 32level
PT15: H Grayscale 64level	PT16: LOD bist pattern	PT1D: sub-pixel checker	PT1E: 2-line sub-pixel checker	PT1F: 2-line sub-pixel checker

3.4 Lvds data mapping type could be set by internal registers, and 8-bit data sequence is shown as following table

Channel No.	Data No.	8-bit LVDS TYPE	
		NS	**JEIDA**
0	Bit-0	R0	R2
	Bit-1	R1	R3
	Bit-2	R2	R4
	Bit-3	R3	R5
	Bit-4	R4	R6
	Bit-5	R5	R7
	Bit-6	G0	G2
1	Bit-0	G1	G3
	Bit-1	G2	G4
	Bit-2	G3	G5
	Bit-3	G4	G6
	Bit-4	G5	G7
	Bit-5	B0	B2
	Bit-6	B1	B3
2	Bit-0	B2	B4
	Bit-1	B3	B5
	Bit-2	B4	B6
	Bit-3	B5	B7
	Bit-4	-	-
	Bit-5	-	-
	Bit-6	DE	DE
3	Bit-0	R6	R0
	Bit-1	R7	R1
	Bit-2	G6	G0
	Bit-3	G7	G1
	Bit-4	B6	B0
	Bit-5	B7	B1
	Bit-6	-	-

Note:The first pixel is odd.

3.3 Backlight Electrical / Optical Characteristics

3.3.1 backlight connector

"CN2 : PH1.0-6P

Pin#	Signal Name
1	VDD-
2	VDD-
3	VDD+
4	VDD+
5	VDD-
6	VDD-

3.3.2 LED Bar

Parameter	Symbols	Min	Typ	Max	Unit
Forward Voltage (one circuit)	VF	2.8	-	3.6	MHz
Reverse Current (one circuit)	IR	-	-	10	μA
Forward Current	IF	-	90	120	Ma
Chromaticity Coordinates	X	0.285	0.291	0.297	
	Y	0.254	0.270	0.277	
Lumen	¢	20	22	24	LM
Viewing Angle	2θ1/2	-	120	-	Deg.
Number Of LED	Pcs	-	80	-	Pcs
Operation Voltage(LB)	VLB	56	-	64	V
Operation Current(LB)	ILB	-	240	-	mA
Power Consumption	PLB	13.44	-	15.36	W

3.4. Timing spec

The input signal timing specifications are shown as the following table and timing diagram

		Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock Frequency		F_{CLK}	45	74.25	95	MHZ	
Vertical Term	Frame Rate	F	40	60	76	HZ	
	Total	Tv	1115	1125	1240	T_H	
	Active Display	T_{VD}		1080		T_H	
	Blank	T_{VB}	35	45	160	T_H	
Horizontal term	Total	T_H	1010	1100	1250	T_{CLK}	
	Active Display	T_{HD}		960		T_{CLK}	
	Blank	T_{HV}	40	140	230	T_{CLK}	

Attention:

The module is operated in DE only mode ,H sync and V sync input signal have no effect on normal operation.

Note(1)Please make sure the range of pixel clock follows the following equations:

FCLK　(max) ≥Fmax × Tv × TH
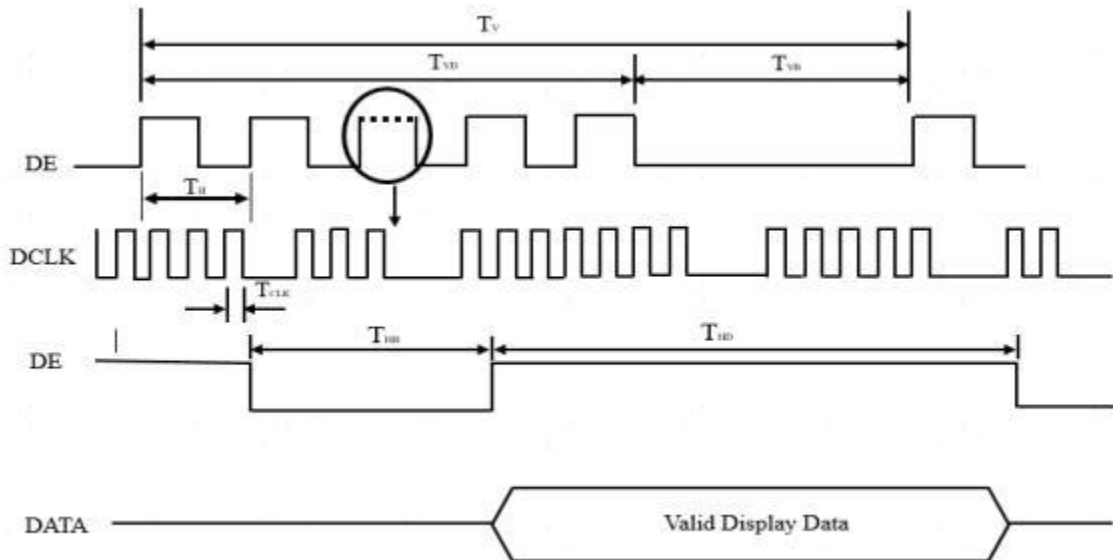
Fig 3.4.1 Signal timing diagram

3.5 Power On/Off Sequence

To prevent a latch-up or DC operation of the Open cell, the power on/off sequence should be as the diagram below.
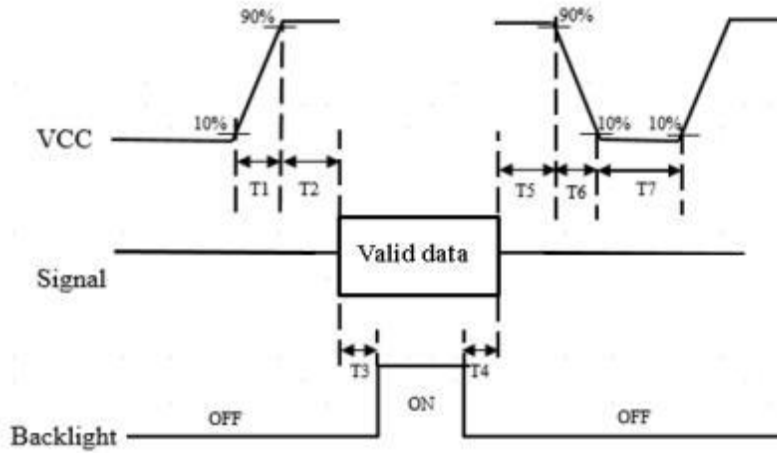
Fig.3.5.1 Power on/off sequence

Parameter	Values			Unit
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	30	50	ms
T3	450	-	-	ms
T4	100	250	-	ms
T5	0	20	50	ms
T6	0.1	-	100	ms
T7	1000			ms

Note:

(1)   The supply voltage of the external system for the module input should be the same as the definition .

(2)   To avoid some abnormal display noise, we suggest "Vcc falling time" to follow "T6" definition.

(3)   In case of Vcc is off level, please keep the level of input signals on the low or keep high impedance.

3.6 Flicker adjustment

(1) The power sequence specifications are shown as the following table and diagram：
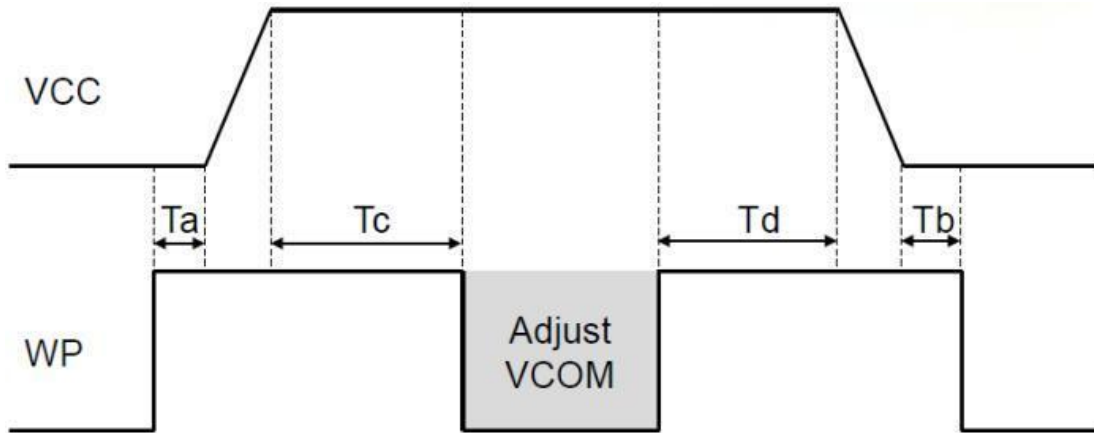
Parameters	Values			Units
	Min.	Typ.	Max.	
Ta	50	-	100	ms
Tb	50	-	100	ms
Tc	1000	-	-	ms
Td	1000	-	-	ms

(2) Digital VCOM Modify Flow
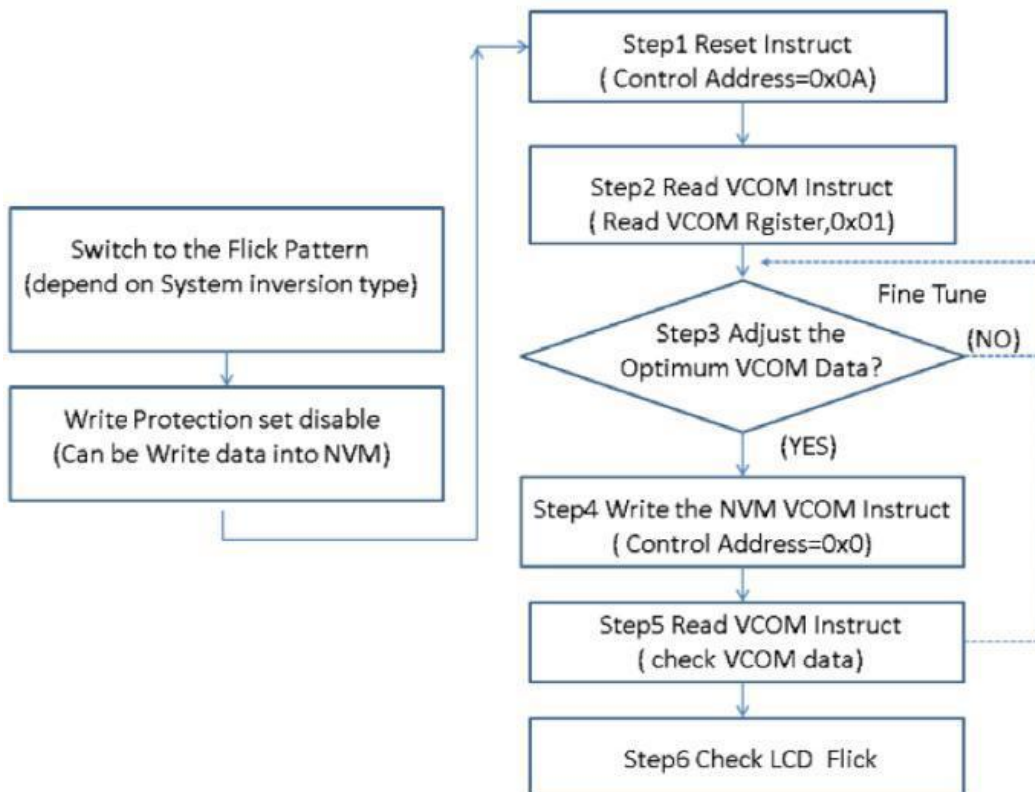
A.Switch to the Flicker Pattern (EX: Dot inversion pattern)
(EX: Dot inversion pattern)
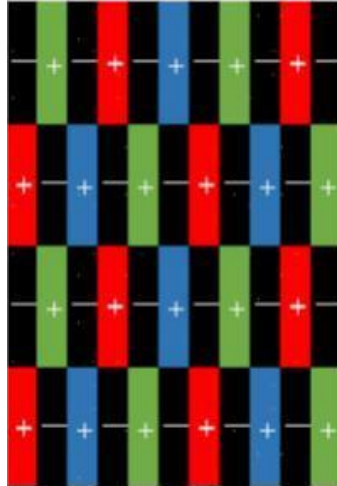
B. WP (Write Protect) Disable

Because that the HA5901A with NVM protection function. It is necessary to disable the NVM protection first before the HA5901A execute write to NVM instruction. See the figure below for WP Table.

P-Gamma Type	Pin	nWR	Write-Protection NVM Function	Description
HA5901A01	16	H	Enable (can't write to NVM)	Enable/disable Write-Protection. (writes data in nonvolatile memory)
		L	Disable (can be write to NVM)	
HA5901A02 HA5901A03	12	H	Disable (can be write to NVM)	
		L	Enable(can't write to NVM)	

C . About VCOM Adjustment(I2C Bus Format)

S indicates START
P indicates STOP
Aindicates ACKNOWLEDGEMENT
NA indicates NO ACKNOWLEDGEMENT
SR indicates REPEAT START
R indicates READ
W indicates WRITE

Step1 Dump the VCOM NVM data to VCOM Register (Reset Command)

*Device Address is 0x74 (7 bit define)

S	Slave Address	W	A	Index Address 0	A	Control data(0x12)	A	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 0		0 0 0 1 0 0 1 0		
	0xE8			0x00		0x12		
	Device Address + W			Control Address		Reset + OUT_EN		

Step2 Read the VCOM data from VCOM Register (Read the VCOM register)

*DVCOM Data = 7Bits

S	Slave Address	W	A	Index Address 1	SR	Slave Address	R	A	DVCOM	NA	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 1		1 1 1 0 1 0 1 1			X X X X X X X X		
	0XE8			0X01		0XE9					
	Device address + W			VCOM Address		Device address + R			Data		

Step3 Adjust VCOM

*DVCOM data = 7Bits

S	Slave Address	W	A	Index Address 1	A	DVCOM Data	A	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 1		0000000X~1111111X		
	0XE8			0X01		0x00~0xFE (bit 0 is reserve bit)		
	Device address + W			VCOM Address		VCOM value		

Step4 Write the optimum VCOM data into NVM

(After the VCOM adjustment, write the DVCOM data of register to VCOM NVM)

S	Slave Address	W	A	Index Address 0	A	Control Data(0x0A)	A	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 0		0 0 0 0 1 0 1 0		
	0xE8			0x00		0x0A		
	Device Address + W			Control Address		Write DAC to NVM + OUT_EN		

Step5 Dump the VCOM NVM data to VCOM Register (Reset Command)

(Check the final DVCOM Data)

*Device Address is 0x74 (By 7bit define)

S	Slave Address	W	A	Index Address 0	A	Control Data(0x12)	A	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 0		0 0 0 1 0 0 1 0		
	0xE8			0x00		0x12		
	Device Address + W			Control Address		Reset + OUT_EN		

Step6 Read the VCOM data from VCOM Register (Read the VCOM register)

*DVCOM Data = 7Bits

S	Slave Address	W	A	Index Address 1	SR	Slave Address	R	A	DVCOM	NA	P
	1 1 1 0 1 0 0 0			0 0 0 0 0 0 0 1		1 1 1 0 1 0 1 1			X X X X X X X X		
	0XE8			0X01		0XE9					
	Device address + W			VCOM Address		Device address + R			Data		

D. Interval times of Step to Step
The interval times must follow below figure.
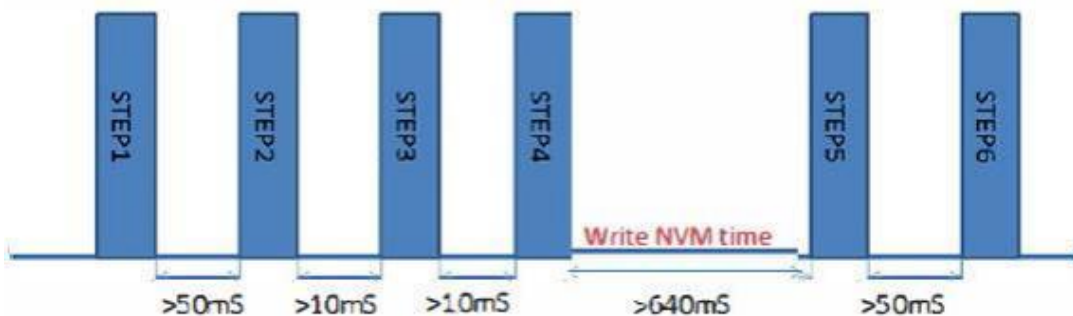
(3) I2C Electrical Characteristics spec

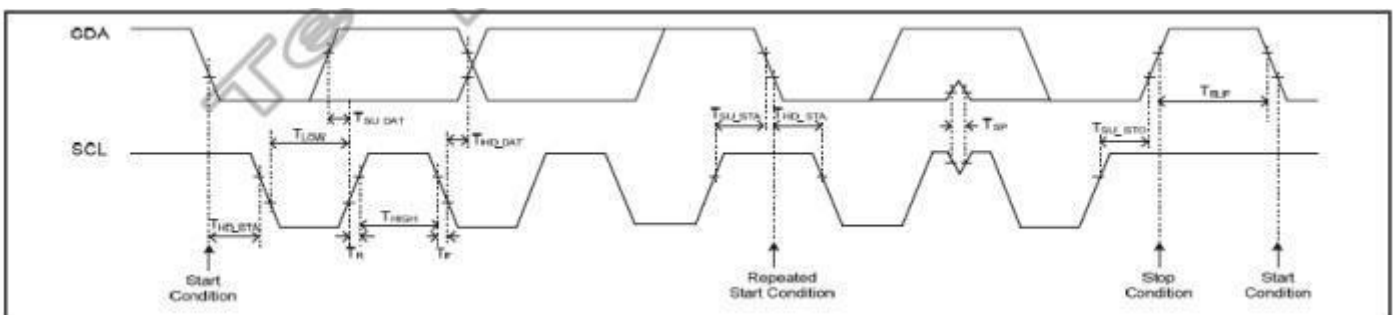(VDDA=18V, VDDD=2.9V, VSSA=VSSD=0V, no load, T_A=TMIN to TMAX, unless otherwise noted. Typical values are at T_A=+25°C.)

Parameter	Description	Condition	Spec.			Unit
			Min.	Typ.	Max.	
I²C						
V_{IL}	Logic-input low input	SCL, SDA	-	-	0.3*VDDD	V
V_{IH}	Logic-input high input	SCL, SDA	0.7*VDDD	-	-	V
F_{SCL}	Serial-clock frequency	-	1	-	400	KHz
T_{HIGH}	SCL pulse-width high	-	0.6	-	-	µs
T_{LOW}	SCL pulse-width low	-	1.2	-	-	µs
T_{SU_DAT}	Data setup time	-	100	-	-	ns
T_{HD_DAT}	Data hold time	-	0	-	900	ns
T_{M_I2C}	I²C mask time	-	7.36	8.5	9.82	ms
T_R	SDA and SCL receiving rise time	-	-	-	1000	ns
T_F	SDA and SCL receiving fall time	-	-	-	300	ns
T_F	SDA and SCL input capacitance	-		5		pF
T_{SU_STA}	Setup time for a repeated START condition	-	0.6	-	-	µs
T_{HD_STA}	Hold time (Repeated) START condition	10% SDA to 90% SCL	0.6	-	-	µs
T_{SU_STO}	Setup time for STOP condition	-	0.6	-	-	µs
T_{SP}	Pulse width of suppressed spike	-	0	-	50	ns
T_{BUF}	Bus free time between STOP and START conditions	-	4.7	-	-	µs

4 Optical Characteristics

4.1 Test Condition

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25 ± 2	℃
Ambient Humidity	Ha	50 ± 10	%RH
Supply Voltage	Vcc	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Input Voltage	V_{LED}	58.3	V
LED Input Current	I_{LED}	240	mA
Power Consumption	Pw	14	W

4.2 Optical Characteristics

The relative measurement methods of optical characteristics are shown as below.

The following items should be measured under the test conditions described in 4.1
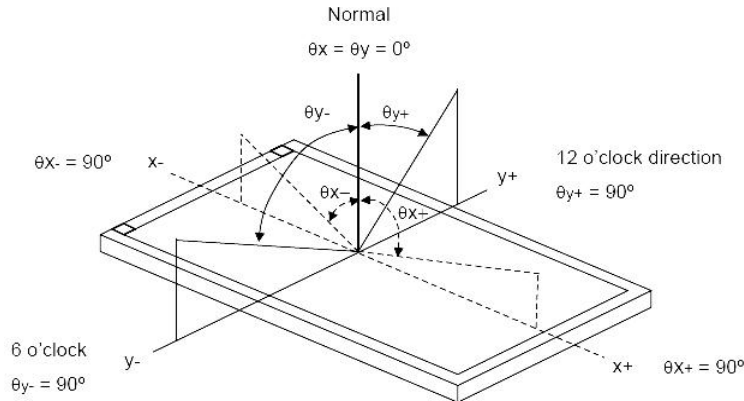
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		—	1000	—	—	—
Response Time		TL		—	14	25	ms	Note 3
Brightness uniformity		BU		70	75	—	—	Note 2
Center Luminance of White		Lc		220	250	—	cd/m2	—
The color chromatic	Red	Rx	θx=0,θy=0, viewing normal angle	Typ. -0.03	0.660	Typ. +0.03	—	—
		Ry			0.330		—	—
	Green	Gx			0.330		—	—
		Gy			0.600		—	—
	Blue	Bx			0.148		—	—
		By			0.057		—	—
	White	Wx			0.313		—	—
		Wy			0.329		—	—
Viewing Angle	Horizontal	θx+	CR≧10	—	89	—	Deg	Note 1
		θx-		—	89	—		
	Vertical	θy+		—	89	—		
		θy-		—	89	—		

Note 1: The definition of viewing angle

Note 2: Definition of luminance , CR measured positions and brightness uniformity

(a) Measure White luminance on the below 9 points and take the average value .

(b) CR : measures the same 9 points and take the average value .The Definition of Contrast Ratio   is as follows :
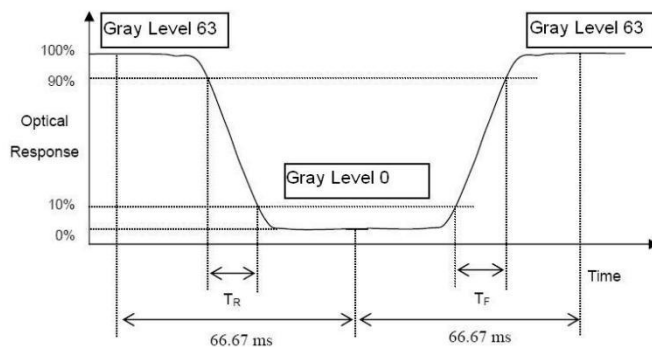
CR = ON(white L63)Luminance / OFF (Black L0)Luminance

(c) The definition of White Vibration

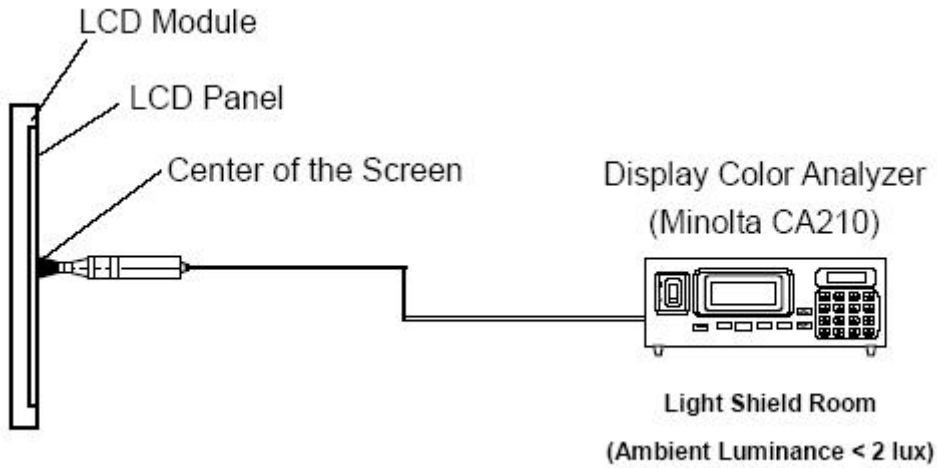$$\frac{\text{The minimum brightness of} \quad 9 \text{ dot}}{\text{The maximum brightness of} \quad 9 \text{ dot}} \times 100\%$$
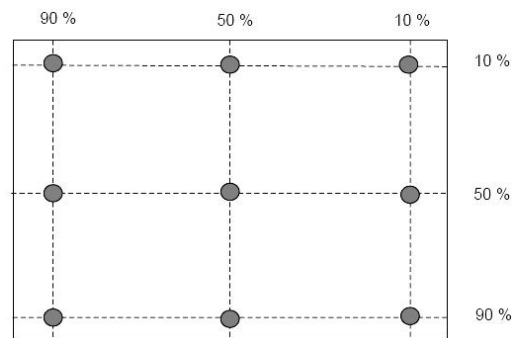
Note 3:Definition of Response Time (TR, TF):

Note 4: The measure method

(a) : The measurement point is the center of the active area except for the measurement of Luminance Uniformity

(b) : Photometer :CA-210

5.0 Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃，80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃，50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃，300hours	
High Temperature Storage (HTS)	Ta= 60℃，300hours	
Low Temperature Storage (LTS)	Ta= -20℃，300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction:±X,±Y,±Z(one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electric Static Discharge)	Contact Discharge: ± 4KV, 150pF(330) 1sec, 8 points, 25 times/ point.	2
	Air Discharge: ± 8KV, 150pF(330) 1sec 8 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: EN61000-4-2, ESD class B: Certain performance degradation allowed

      No data lost

      Self-recoverable

      No hardware failures.

6.0 Shipping Label

6.1 Panel Label

Model   No: M238HCT02 B1F
OC PN   : PN238CT02-14

ABCDEFGHIJKLMNHIJK

RoHS

6.2 Carton Label

ABCDEFGHIJKLMN

Model No:(型号)：M238HCT02 B1F

OC PN   :   PN238CT02-14

QTY(数量)   : 10 PCS/CTN

N.W(净重)   :   KG

G.W(毛重)   :   KG

7. Packaging

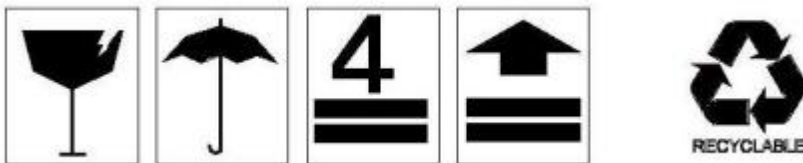### 9.1 Carton(internal package)

(1)Packaging Form

(2) Packaging Method

(TBD)

Note 1)   Acceptable number of piling : 10 sets

7.2 Packing Mark

8. PRECAUTION

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

1   Do not apply rough force such as bending or twisting to the module during assembly.
2   To assemble or install module into user's system can be in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
3   It's not permitted to have pressure or impulse on the module because the LED panel and Backlight will will be damaged.
4   Always follow the correct power sequence when LED module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
5   Do not pull the I/F connector in or out while the module is operating .
6   Do not disassemble the module. Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very
7   soft and easily scratched.
8   It is dangerous that moisture come into or contacted the LED module, because moisture may damage LED module when it is operating.
9   High temperature or humidity may reduce the performance of module. Please store LED module within the specified storage conditions.
10 When ambient temperature is lower than 10 ℃ may reduce the display quality. For example, the response time will become slowly.

8.2 SAFETY PRECAUTIONS

1   It is dangerous that moisture come into or contacted the LED module, because the moisture may damage LED module when it is operating.
2   If the liquid crystal material leaks from the panel,it should be kept away from the eyes or mouth, in case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
3   After the modlule's end of life, it is not harmful in case of normal operation and storage.

9. Outline dimensions

A-A:527.04*296.46

LVDS CONNECTOR

PH 1.0 6PIN