
	PRODUCTION SPECIFICATION OF TFT LCD MODULE	Model No: M215CB04 V3
		OC PN: SG2151B04-3

**PRODUCTION SPECIFICATION
OF TFT LCD MODULE**

Model No. : M215CB04 V3

OC PN: SG2151B04-3

CUSTOMER	
CONFIRMED BY	
APPROVED BY	

PREPARED BY	
CONFIRMED BY	

	PRODUCTION SPECIFICATION OF TFT LCD MODULE	Model No: M215CB04 V3
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Date	Rev.	Page	Old Description	New Description	Remark
2023.03.15	1.0	All	The specification was first issued		

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

DLM215CB04 V3 is a TFT LCD module which used CSOT SG2151B04-3 open cell with 2ch-LVDS interface. This open cell is a transmissive type display operating in the normally black mode. It supports 1920 * 1080 FHD resolution and can display up to 16.7M colors (8bit). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in vertical stripe.

This open cell dedicates for LCD TV & Monitor & PID products and provides excellent performance which includes high brightness, ultra wide viewing angle, high color saturation and high color depth. CSOT open cell comply with RoHS for identification.

1.2 General Specifications

Item	Specification	Unit	Note
Active Area	476.64 (H) * 268.11 (V)	mm	
Cell Size	487.54 (H) * 279.684 (V) * 1.335 (D)	mm	
Weight	1.7	kg	Max.
Driving Scheme	a-Si TFT Active Matrix	-	
Number of Pixels	1920 * 1080	pixel	
Pixel Pitch (Sub Pixel)	0.08275*0.24825	mm	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7 M	color	8bit
Display Mode	Transmissive Mode, Normally Black		
Module Brightness	250	Cd/m ²	
Color Chroma	R = (0.644, 0.336)		Typical value measured at DL BLU
	G = (0.310, 0.616)		
	B = (0.153, 0.050)		
	W = (0.310, 0.330)		
Contrast Ratio	4000:1(Typ.)		
View Angle (CR 10)	+89/-89 (H), +89/-89 (V) (Typ.)		
Surface Treatment	Anti-glare, Haze 2%, Hard Coating (3H)		

1.3 Mechanical Specification

Item		Min	Typ	Max	Unit	Note
Weight		-100	1700	+100	g	-
Module Size	Horizontal(H)	(TYP)-0.5	495.60	(TYP)+0.5	mm	1
	Vertical (V)		292.20		mm	
	Depth(D)		9.50		mm	

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2. Absolute Maximum Ratings

2.1 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[oC]	Note 3
Glass surface temperature (operation)	TGS	0	+65	[oC]	Note 3, Note 4
Operation Humidity	HOP	5	90	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[oC]	
Storage Humidity	HST	5	90	[%RH]	

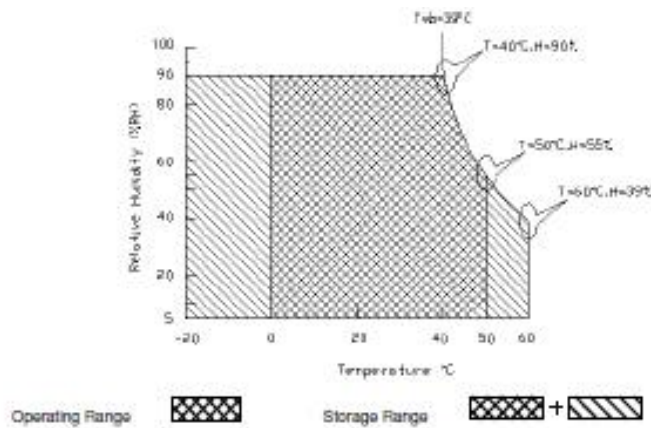
Note 1: With in Ta (25C)

Note 2: Permanent damage to the device may occur if exceeding maximum values.

Note 3: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max
2. Max wet-bulb temperature at 39

Note 4: Function Judged only



2.2 Backlight Unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LED operation Voltage	V_{led}	50.4	-	64.8	V_{led}	
LED operation Current	I_{led}	-	240	-	mA	(1)
BackLight Power	P_{BL}	12.10	-	15.55	W	
Lift time	Lt	30000	40000	-	Hrs	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal operating Conditions.

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3. ELECTRICAL CHARACTERISTICS

3.1 Open Cell Power Consumption (TA = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note	
		Min.	Typ.	Max.			
Power Supply Voltage	VCC	4.5	5	5.5	V	(1)	
Rush Current	IRUSH	-	-	3	A	(2)	
Power Supply Current	White Pattern	ICC	-	0.35	0.46	A	(3)
	Horizontal Stripe	ICC	-	0.52	0.68	A	
	Black Pattern	ICC	-	0.33	0.43	A	

Note:

(1) The ripple voltage should be controlled less than 10% of VCC.

(2) Measurement condition: VCC = 5V, Rising time = 470µs.

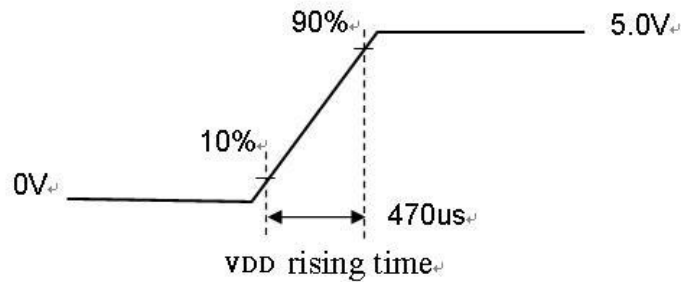


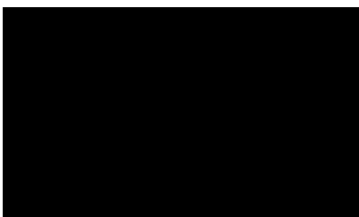
Fig. 3.1 VCC rising time condition

(3) Measurement condition: VCC = 5V, Ta = 25 ± 2°C, F = 60 Hz. The test patterns are shown as below.

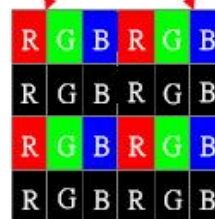
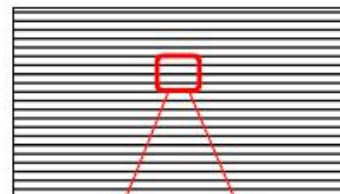
A. White Pattern



B. Black Pattern



C. Horizontal Pattern



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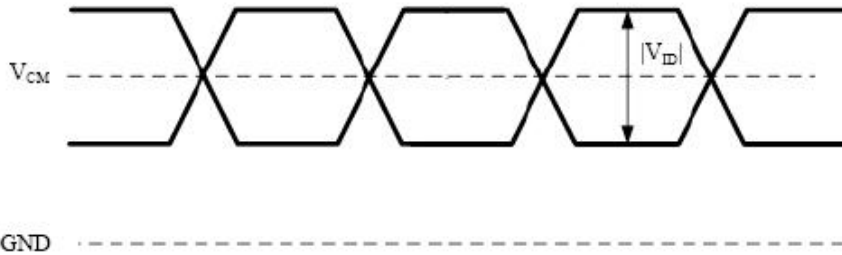
3.2 LVDS Characteristics

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	VTH	+100	-	-	(1)
	Differential Input Low Threshold Voltage	VTL	-	-	-100	
	Common Input Voltage	VCM	1.0	1.2	1.4	
	Differential Input Voltage	VID	100	-	600	
	Terminating Resistor	RT	87.5	100	112.5	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V
	Input Low Threshold Voltage	VIL	0	-	0.7	V

Note:

- (1) The product should be always operated within above ranges.
- (2) The LVDS input signal has been defined as follows:

Single end Signals



Differential Signal

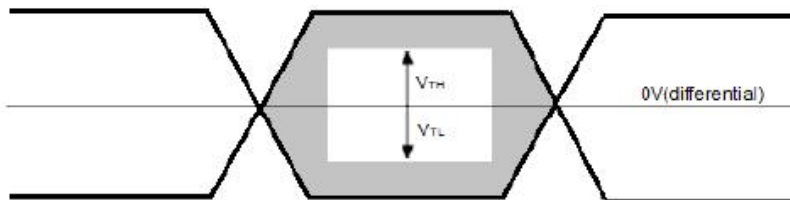


Fig. 3.3 LVDS input signal

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3.3 Temperature Specifications

Parameter	Symbol	Specification			Unit	Recommend test pattern	Note
		Min.	Typ.	Max.			
Surface Temperature	TTCON	-	-	85	°C	Horizontal Pattern	(1)
	TDriver	-	-	115		Horizontal Pattern	(1)
	TPmic	-	-	100		Horizontal Pattern	(1)

Note:

(1) Any point on the IC surface must be less than Max. specification under any condition, If the surface temperature is out of the specification, thermal solutions should be applied to avoid be damaged;

3.4 Driver IC ESD Specification

The Electro-Static Discharge tolerance of Source COF IC and Gate COF IC is +-2KV tested by ESD Gun. Especially if the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid be damaged,

as shown in Fig.3.4 and Fig.3.5.

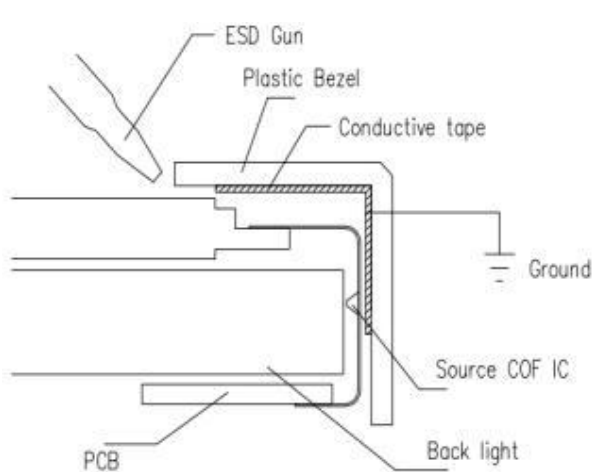


Fig. 3.4 Source COF IC ESD protection

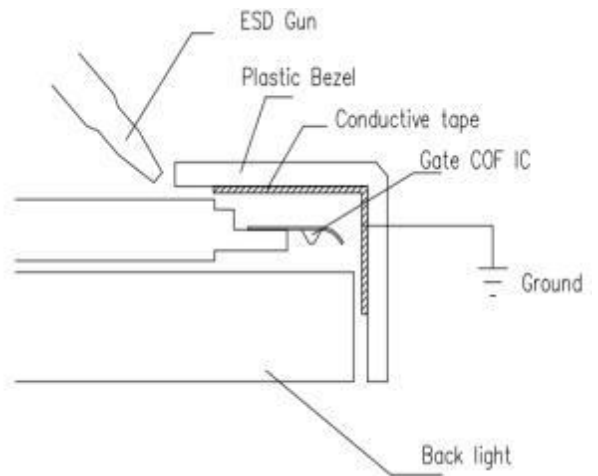


Fig. 3.5 Gate COF IC ESD

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4. Input Terminal Pin Assignment

4.1 Interface Pin Assignment

CN1: 1-301223-0 (XINDAYITONG) or equivalent (see Note (1))

PIN #	Symbol	Description	REMARK
1	RO[0]N	Odd LVDS Signal -	
2	RO[0]P	Odd LVDS Signal +	
3	RO[1]N	Odd LVDS Signal -	
4	RO[1]P	Odd LVDS Signal +	
5	RO[2]N	Odd LVDS Signal -	
6	RO[2]P	Odd LVDS Signal +	
7	GND	Ground	
8	ROCLK-	Odd LVDS Clock -	
9	ROCLK+	Odd LVDS Clock +	
10	RO[3]N	Odd LVDS Signal -	
11	RO[3]P	Odd LVDS Signal +	
12	RE[0]N	Even LVDS Signal -	
13	RE[0]P	Even LVDS Signal +	
14	GND	Ground	
15	RE[1]N	Even LVDS Signal -	
16	RE[1]P	Even LVDS Signal +	
17	GND	Ground	
18	RE[2]N	Even LVDS Signal -	
19	RE[2]P	Even LVDS Signal +	
20	RECLK-	Even LVDS Clock -	
21	RECLK+	Even LVDS Clock +	
22	RE[3]N	Even LVDS Signal -	
23	RE[3]P	Even LVDS Clock +	
24	GND	Ground	
25	WP	Write Protect (High: Write Enable, Low or Open: Write Disable)	(2)
26	SCL	I2C Serial Clock (for adjust VCOM)	(2)
27	SDA	I2C Serial Data (for adjust VCOM)	(2)
28	5V	DC power supply	
29	5V	DC power supply	
30	5V	DC power supply	

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Note:

(1) The direction of pin assignment is shown as below:

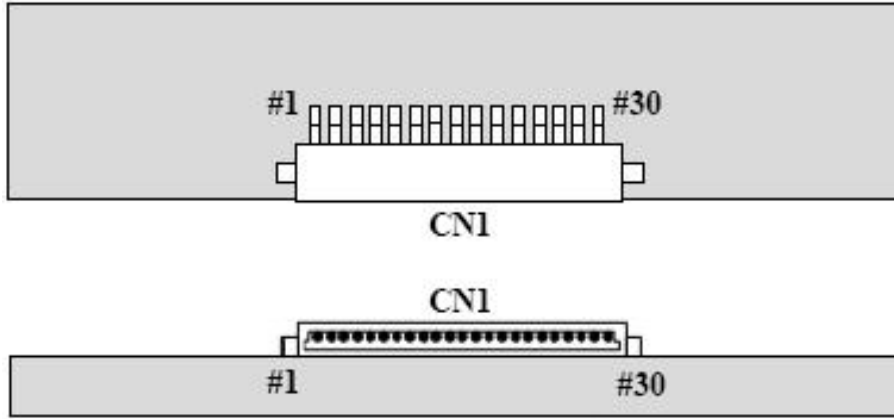


Fig. 4.1 LVDS connector direction sketch map

(2) a. Please let it open (Do not line out from PCBA connector) if it do not used.

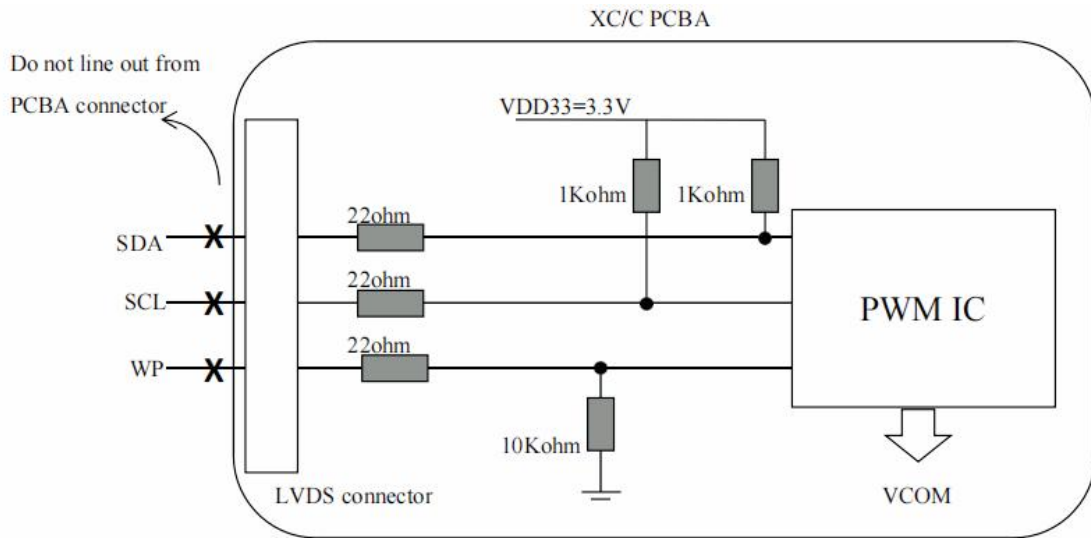
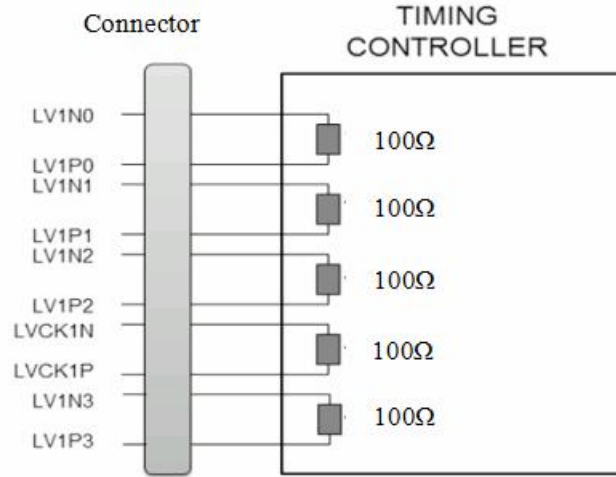


Fig. 4.2 WP/SDA/SCL PCBA set

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4.2 Block Diagram of Interface

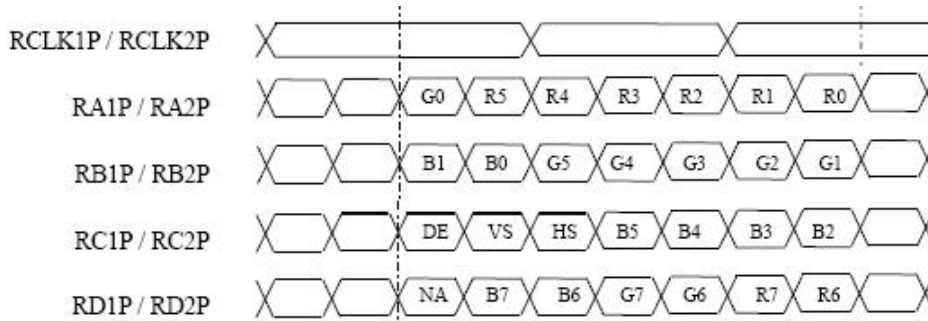


Attention:

- (1) This open cell uses a 100 ohms (Ω) resistor between positive and negative lines of each receiver input.
- (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line respectively.

4.3 LVDS Interface

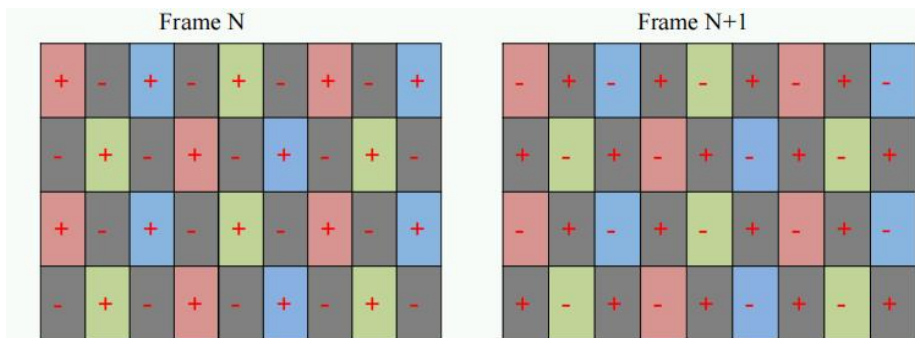
4.3.1 VESA Format



4.4 Flicker Pattern

Flicker should be adjusted by the Dot on/off pattern, where are displayed alternately at vertical line. (Dot inversion)

Dot on/off pattern



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4.5 Backlight Electrical / Optical Characteristics

4.5.1 backlight connector

"CN2 : BH3.5-2P

Pin#	Signal Name
1	VDD- (Black)
2	VDD+ (Red)

4.5.2 LED Bar

Parameter	Symbols	Min	Typ	Max	Unit
Forward Voltage (one circuit)	VF	2.8	-	3.6	MHz
Reverse Current (one circuit)	IR	-	-	10	μA
Forward Current	IF	-	60	100	Ma
Chromaticity Coordinates	X	0.247	0.267	0.287	
	Y	0.222	0.242	0.262	
Lumen	ç	20	22	24	LM
Viewing Angle	2θ1/2	-	120	-	Deg.
Number Of LED	Pcs	-	72	-	Pcs
Operation Voltage(LB)	VLB	50.4	-	64.8	V
Operation Current(LB)	ILB	-	240	-	mA
Power Consumption	PLB	12.096	-	15.552	W
Wire length	Lw	-	500	-	mm

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5. Interface Timing

5.1 Timing Table (DE Only Mode)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	Fclk (=1/Tclk)	59.4	74.25	92.8	MHz	(1) (2)
	Input cycle to cycle jitter	Trcl	-	-	200	ps	(3)
	Spread spectrum modulation range	Fclk_mod	Fclk-2 %	-	Fclk+2 %	MHz	(4)
	Spread spectrum modulation frequency	FSSM	60	-	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	TRSM	-400	-	400	ps	(5)
Vertical Active Display Term	Frame Rate	F	48	60	75	Hz	
	Total	TV	1092	1125	1380	TH	TV = TVD +TVB
	Display	TVD	1080				
	Blank	TVB	12	45	300	TH	
Horizontal Active Display Term	Total	TH	1046	1100	1174	TCLK	TH = THD + THB
	Display	THD	960				
	Blank	THB	86	140	214	TCLK	

Note:

(1) The TFT LCD open cell is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

(2) Please make sure the range of pixel clock follows the following equations:

$$Fclk(max) \geq Fmax \times Tv \times Th \quad Fmin \times Tv \times Th \geq Fclk(min)$$

Main frequency Max is 96Mhz without spread spectrum

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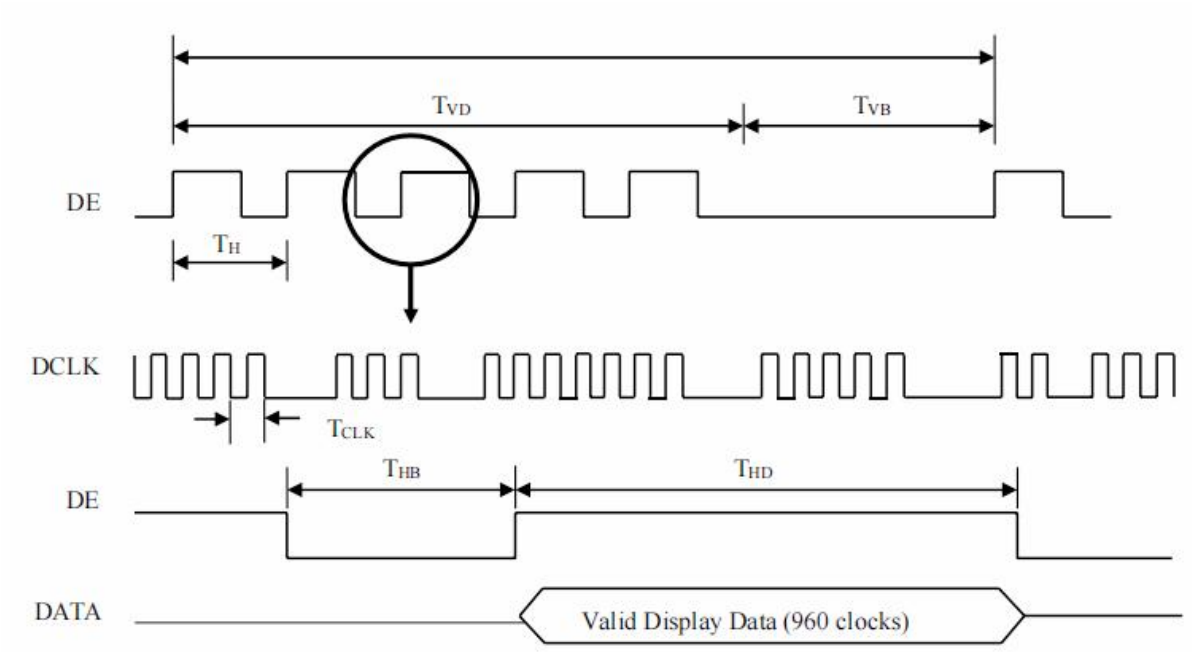


Fig. 5.1 Interface signal timing diagram

(3) The input clock cycle-to-cycle is defined as below figures.

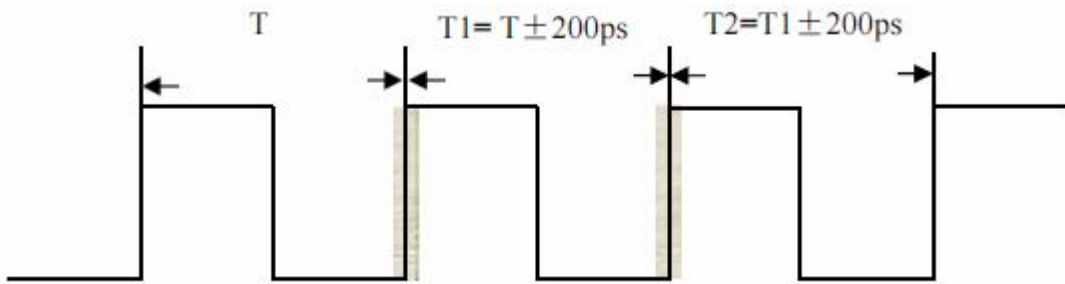


Fig. 5.2 Jitter

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(4) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure. The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM.

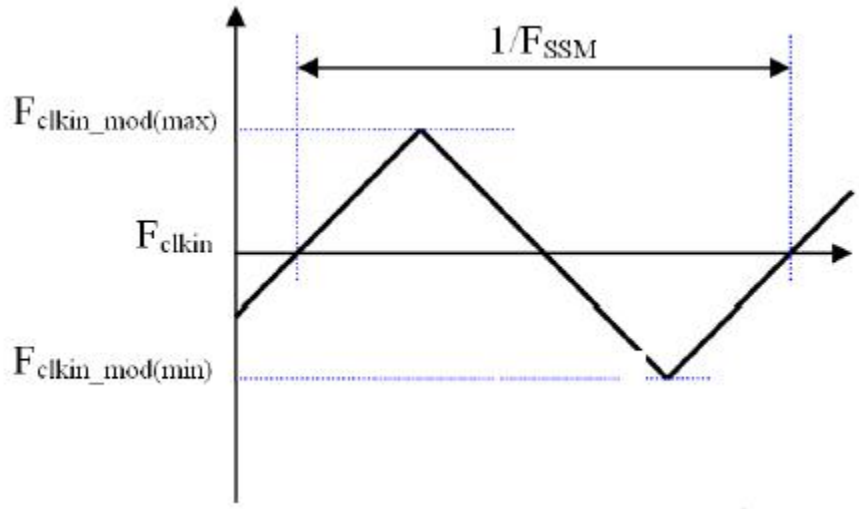


Fig. 5.3 SSCG

(5) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

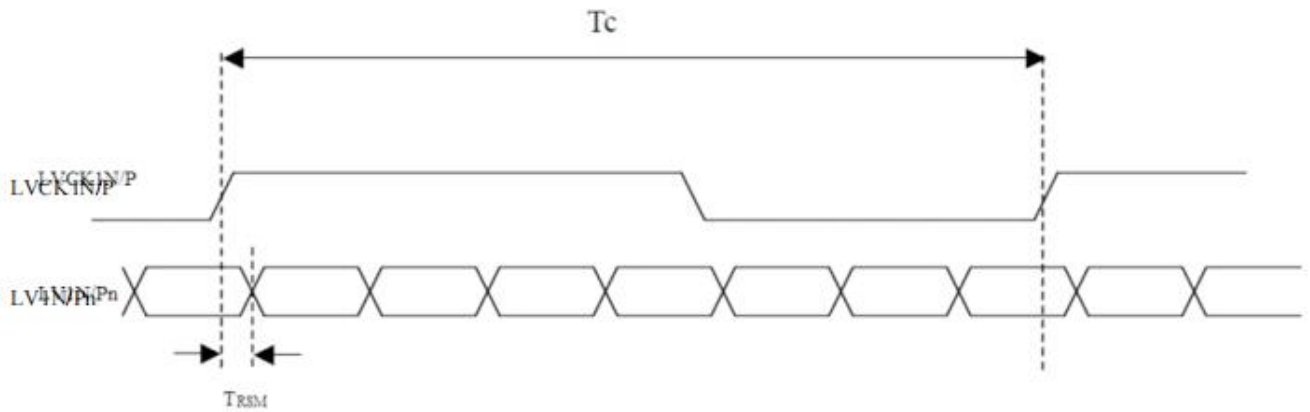


Fig.5.4 LVDS receive interface timing diagram

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5.2 Power On/Off Sequence

To prevent a latch-up or DC operation of the Open cell, the power on/off sequence should be as the diagram below.

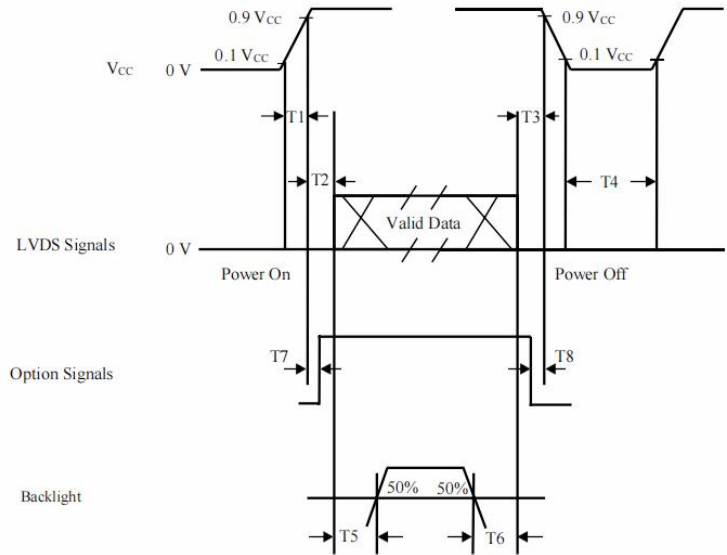


Fig.5.5 Power on/off sequence

Parameter	Values			Unit Min.
	Min.	Typ.	Max.	
T1	0.5	-	10.0	ms
T2	0.0	-	50	ms
T3	0.0	-	50	ms
T4	1000.0	-	-	ms
T5	500.0	-	-	ms
T6	100.0	-	-	ms
T7	-	-	T2	ms
T8	-	-	T3	ms

Attention:

- (1) The supply voltage of the external system for the open cell input should follow the definition of VCC.
- (2) When the customer’s backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case that VCC is in off level, please keep the level of input signals on the low or high impedance. If $T2 < 0$, that may cause electrical over stress.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

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6 Optical Characteristics

6.1 Test Condition

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25 ± 2	°C
Ambient Humidity	Ha	50 ± 10	%RH
Supply Voltage	Vcc	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Input Voltage	V _{LED}	53.0	V
LED Input Current	I _{LED}	240.0	mA
Power Consumption	Pw	12.7	W

6.2 Optical Characteristics

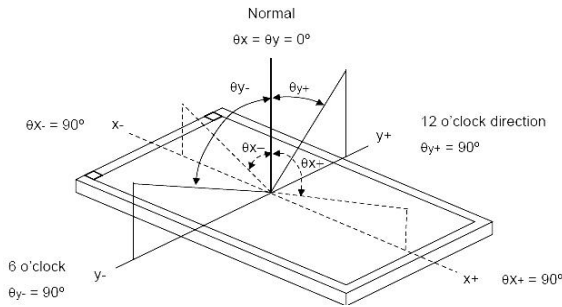
The relative measurement methods of optical characteristics are shown as below.

The following items should be measured under the test conditions described in 6.1

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio	CR	θ _x =0,θ _y =0 , viewing normal angle	—	4000	—	—	—	
Response Time	TL		—	6.5	12	ms	Note 3	
Brightness uniformity	BU		70	75	—	—	Note 2	
Center Luminance of White	L _c		220	250	—	cd/m ²	—	
The color chromatic	Red		R _x	Typ. -0.03	0.644	Typ. +0.03	—	—
			R _y		0.336		—	—
	Green		G _x		0.310		—	—
			G _y		0.616		—	—
	Blue		B _x		0.153		—	—
			B _y		0.050		—	—
	White	W _x	0.310		—		—	
W _y		0.330	—	—				
Viewing Angle	Horizontal	θ _{x+}	CR ≧ 10	—	89	—	Deg	Note 1
		θ _{x-}		—	89	—		
	Vertical	θ _{y+}		—	89	—		
		θ _{y-}		—	89	—		

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Note 1: The definition of viewing angle



Note 2: Definition of luminance, CR measured positions and brightness uniformity

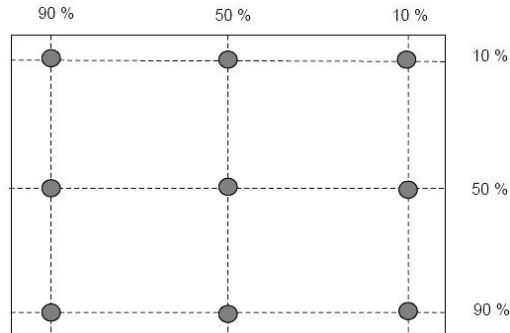
(a) Measure White luminance on the below 9 points and take the average value.

(b) CR : measures the same 9 points and take the average value. The Definition of Contrast Ratio is as follows :

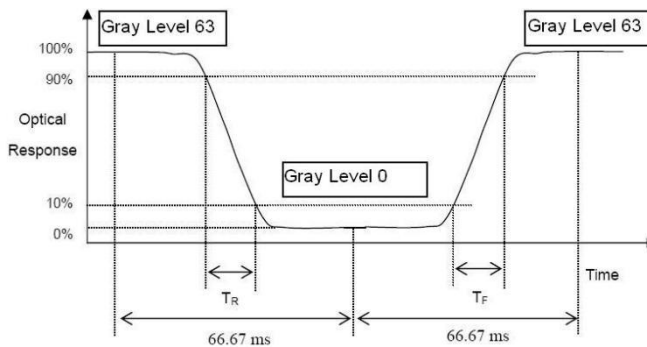
CR = ON(white L63)Luminance / OFF (Black L0)Luminance

(c) The definition of White Vibration

$$\frac{\text{The minimum brightness of 9 dot}}{\text{The maximum brightness of 9 dot}} \times 100\%$$

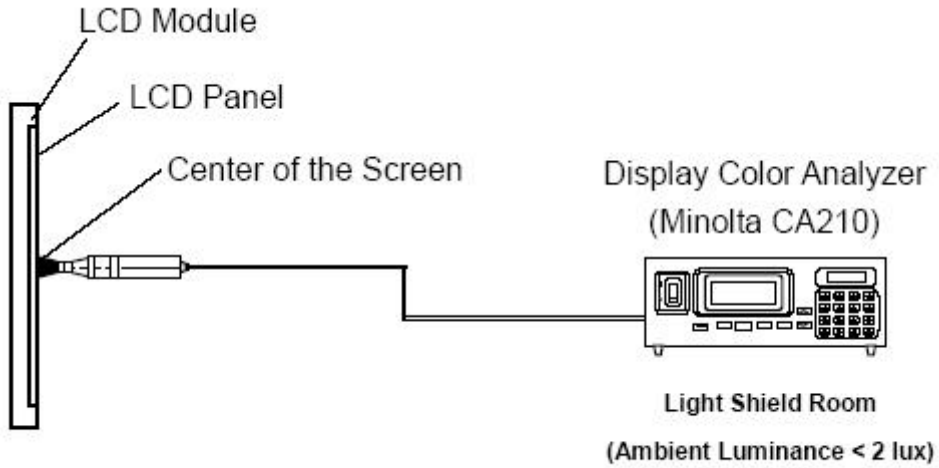


Note 3: Definition of Response Time (TR, TF):



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Note 4: The measure method



- (a) : The measurement point is the center of the active area except for the measurement of Luminance Uniformity
- (b) : Photometer :CA-210

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7.0 Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50°C , 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50°C , 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0°C , 300hours	
High Temperature Storage (HTS)	Ta= 60°C , 300hours	
Low Temperature Storage (LTS)	Ta= -20°C , 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 Grms Wave: Random Frequency: 10 - 200 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction:±X,±Y,±Z(one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 8KV, 150pF(330) 1sec, 8 points, 25 times/ point.	2
	Air Discharge: ± 15KV, 150pF(330) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:18,000 ft Non-Operation:40,000 ft	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: EN61000-4-2, ESD class B: Certain performance degradation allowed

No data lost

Self-recoverable

No hardware failures.

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8.0 Shipping Label

8.1 Panel Label



8.2 Carton Label

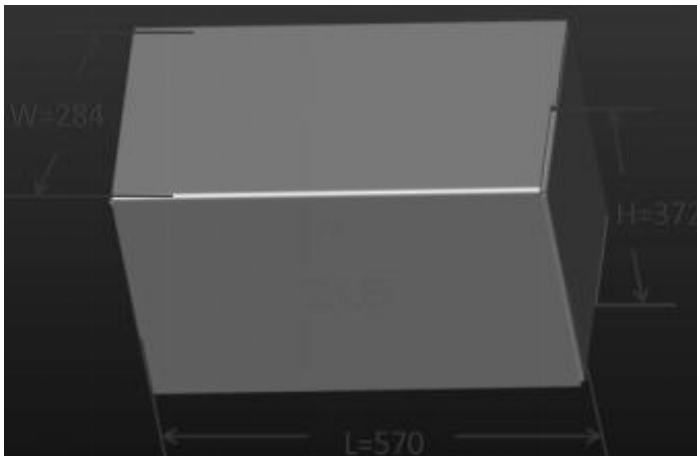
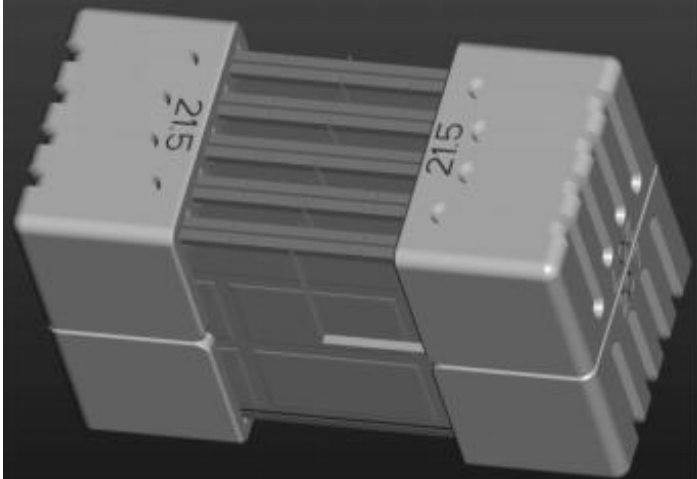


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9. Packaging

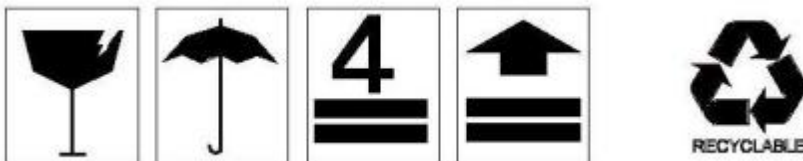
9.1 Carton(internal package)

- (1)Packaging Form
- (2) Packaging Method



Note 1) Acceptable number of piling : 10 sets

9.2 Packing Mark



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10. PRECAUTION

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- 1 Do not apply rough force such as bending or twisting to the module during assembly.
- 2 To assemble or install module into user's system can be in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- 3 It's not permitted to have pressure or impulse on the module because the LED panel and Backlight will be damaged.
- 4 Always follow the correct power sequence when LED module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- 5 Do not pull the I/F connector in or out while the module is operating .
- 6 Do not disassemble the module.
Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very
- 7 soft and easily scratched.
- 8 It is dangerous that moisture come into or contacted the LED module, because moisture may damage LED module when it is operating.
- 9 High temperature or humidity may reduce the performance of module. Please store LED module within the specified storage conditions.
- 10 When ambient temperature is lower than 10 °C may reduce the display quality. For example, the response time will become slowly.

10.2 SAFETY PRECAUTIONS

- 1 It is dangerous that moisture come into or contacted the LED module, because the moisture may damage LED module when it is operating.
- 2 If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth, in case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- 3 After the module's end of life, it is not harmful in case of normal operation and storage.

PRODUCTION SPECIFICATION OF TFT LCD MODULE

Model No:
M215CB04 V3

OC PN: SG2151B04-3

11. Outline dimensions

