PRODUCTION SPECIFICATION
OF TFT LCD MODULE
Model No. : M215HT1 C1
OC PN: PN215CT01-1

CUSTOMER	
CONFIRMED BY	
APPROVED BY	

PREPARED BY	
CONFIRMED BY	

Date	Rev.	Page	Old Description	New Description	Remark
2023.05.10	1.0	All	The specification was first issued		

1.GENERAL DESCRIPTION

1.1 OVERVIEW

The specification is applied to 21.5” model (M215HT1 C1) used HKC PN215CT01-1 opencell. This TFT Liquid Crystal Display open cell supports 1920 x 1080 FHD mode with 16.7M (8bit) colors. This product is with driver ICs and a 30-pins-2ch-LVDS circuit board and built in backlight unit.

1.3 General Specifications

Item	Specifications	Unit	Note
Screen Diagonal	**21.5 inch**	[mm]	Note 1
Active Area	**476.64(H) x 268.11(V)**	[mm]	
Pixels H x V	**1920 x 1080**		
Pixel Pitch	**0.08275(H) x 0.24825 (V)**	[mm]	
Pixel Arrangement	**R.G.B. Vertical Stripe**		
Driver Element	**a-si TFT active matrix**		
Display Mode	**Normally Black**		
Optical Response Time	**7ms (Typ., on/off)**	[msec]	
Display Orientation	**Signal input with“ABC”**		
Support Color	**16.7M colors (6bit with FRC)**		
Surface Treatment	**Anti-Glare, Haze 25%,3H**		
Front bezel	**Black painted**		

1.4 Mechanical Specification

Item		Min	Typ	Max	Unit	Note
Weight		-200	**1700**	+200	g	-
Module Size	Horizontal(H)	(TYP)-1.0	**495.60**	(TYP)+1.0	mm	1
	Vertical (V)		**292.20**		mm	
	Depth(D)		**11.50**		mm	

Note 1: Please refer to the"outline dimension" for more information of back and front outline dimensions.

2. Absolute Maximum Ratings

2.1 Abosolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[oC]	(1)
Operation Humidity	HOP	5	90	[%RH]	(2)
Storage Temperature	TST	-20	+60	[oC]	(3)
Storage Humidity	HST	5	90	[%RH]	(4)

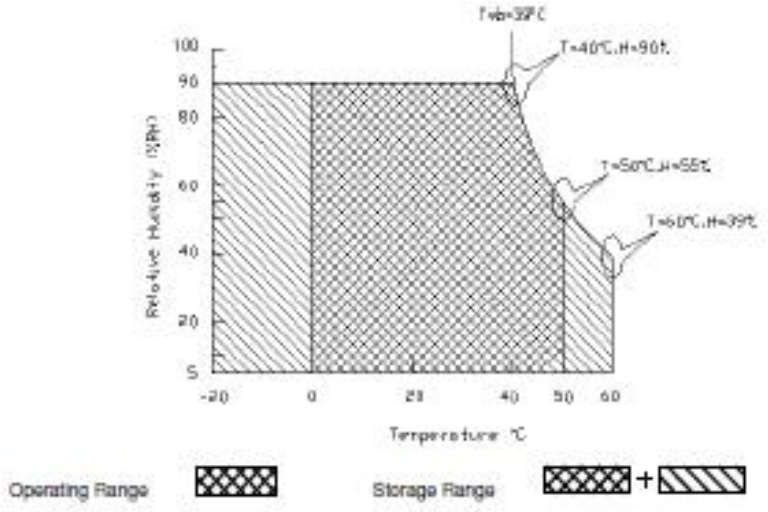
Note 1: With in Ta (25C)

Note 2: Permanent damage to the device may occur if exceeding maximum values

Note 3: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max (≤39C)
2. Max wet-bulb temperature at 39

Note 4: Function Judged only



2.2 Absolute Maximum Ratings

Item	Symbol	Min.	Max.	Unit	Conditions
Power Supply Voltage	VCC	**-0.3**	**6.0**	V	(1)
Input Signal Voltage	Vin	**-0.3**	**3.6**	V	

Note: (1) Within Ta=25±2°C

2.3 Backlight Unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LED operation Voltage	V_{led}	50.4	–	57.6	V_{led}	
LED operation Curent	I_{led}	–	240	–	mA	- (1)
BackLight Power	P_{BL}	12.10	–	13.82	W	(1)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal operating Conditions.

3.0 ELECTRICAL SPECIFICATIONS

3.1Electrical Specifications

3.1.1 Power consumption

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	4.5	5	5.5	V	(2)
Rush Current		I_{RUSH}	-	-	(3)	A	(3)
Power Supply Current	White Pattern	Icc	-	(0.8)	(1.04)	A	(4)
	Horizontal Stripe	Icc	-	(1.28)	(1.66)	A	
	Black Pattern	Icc	-	(0.78)	(1.01)	A	
Power Consumption		P_{LCD}		(4)	(5.2)	Watt	White Pattern

Note:

(1) Ambient temperature: 25 ± 2ºC

(2) The ripple voltage should be controlled under 10% of V_{CC}.

(3) Measurement Conditions: V_{CC} rising time=470μs.

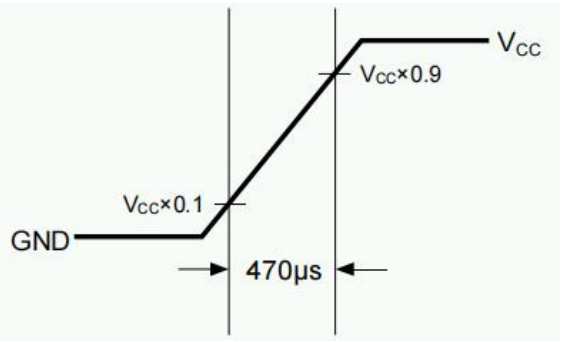
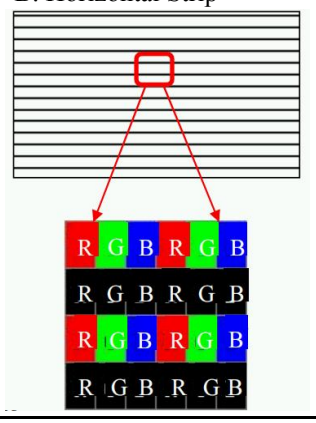


Fig.3.1 V_{CC} rising time condition

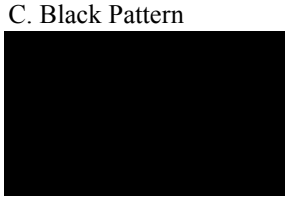
(4) Measurement Conditions: Vcc =12V, Ta = 25 ± 2 ºC, Fv = 60 Hz, whereas the test pattern is shown as below.

A. White Pattern

B. Horizontal Strip



C. Black Pattern



3.1.2 LVDS characteristics

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage	$\|V_{ID}\|$	200	-	600	mV	
	Terminating Resistor	R_T	80	100	120	ohm	
CMOS Interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.6	V	

Note:

(1) The LVDS input signal has been defined as follows:

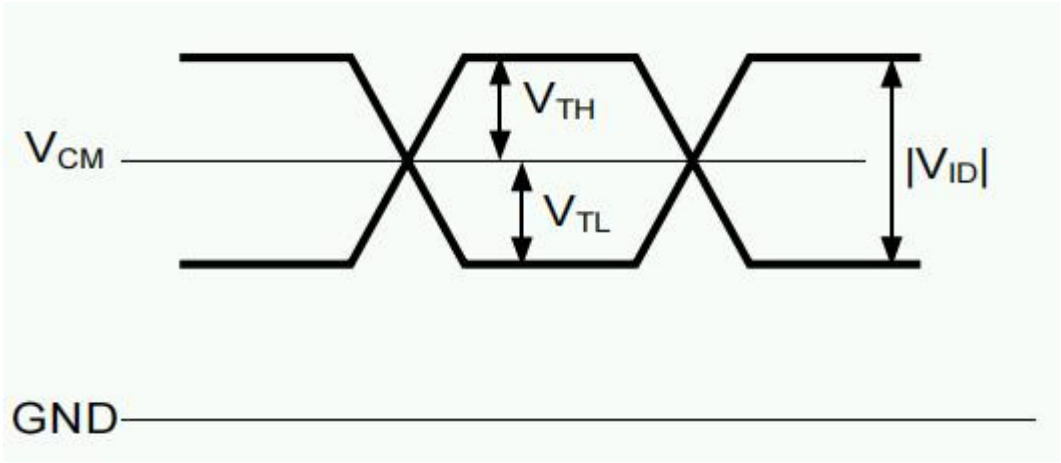


Fig 3.2 Test Test pattern

3.1.3 LVDS format

VESA Format: SELLVDS = L

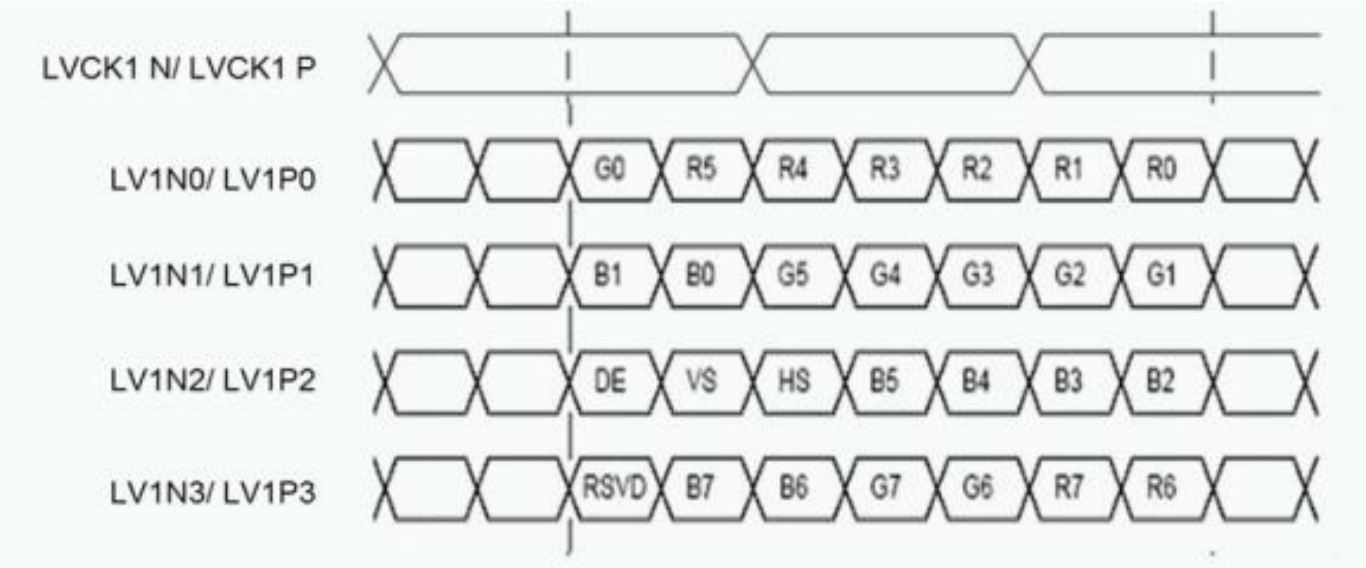


Fig 3.4 VESA format

4.0 INTERFACE CONNECTION.

4.1Interface Pin Assignment

CN1: 3-10122314-0 (XDYT) or equivalent 1mm pitch 30 pin (1)

PIN #	Symbol	DESCRIPTION	REMARK
1	RXO0-	LVDS Odd Data (-)	
2	RXO0+	LVDS Odd Data (+)	
3	RXO1-	LVDS Odd Data (-)	
4	RXO1+	LVDS Odd Data (+)	
5	RXO2-	LVDS Odd Data (-)	
6	RXO2+	LVDS Odd Data (+)	
7	GND	Power Ground	
8	RXOCLK-	LVDS Odd Clock (-)	
9	RXOCLK+	LVDS Odd Clock (+)	
10	RXO3-	LVDS Odd Data (-)	
11	RXO3+	LVDS Odd Data (+)	
12	RXE0-	LVDS Even Data (-)	
13	RXE0+	LVDS Even Data (+)	
14	GND	Power Ground	
15	RXE1-	LVDS Even Data (-)	
16	RXE1+	LVDS Even Data (+)	
17	GNG	Power Ground	
18	RXE2-	LVDS Even Data (-)	
19	RXE2+	LVDS Even Data (+)	
20	RXECLK-	LVDS Even Clock (-)	
21	RXECLK+	LVDS Even Clock (+)	
22	RXE3-	LVDS Even Data (-)	
23	RXE3+	LVDS Even Data (+)	
24	NC	For HKC test only, WP	
25	NC	For HKC test only, SCL	
26	NC	For HKC test only, SDA	
27	NC	For HKC test only, Bist	
28	VDD	Power supply +5.0V	
29	VDD	Power supply +5.0V	
30	VDD	Power supply +5.0V	

Note 1 : This pin should be connected with GND.

Note:

(1) Following finger shows the LVDS pin1 diagram.

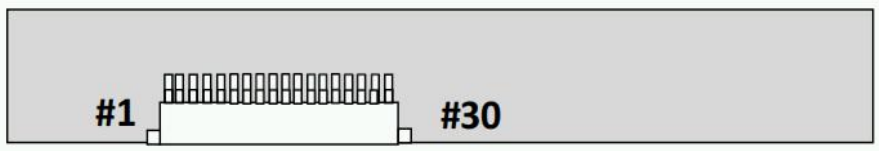
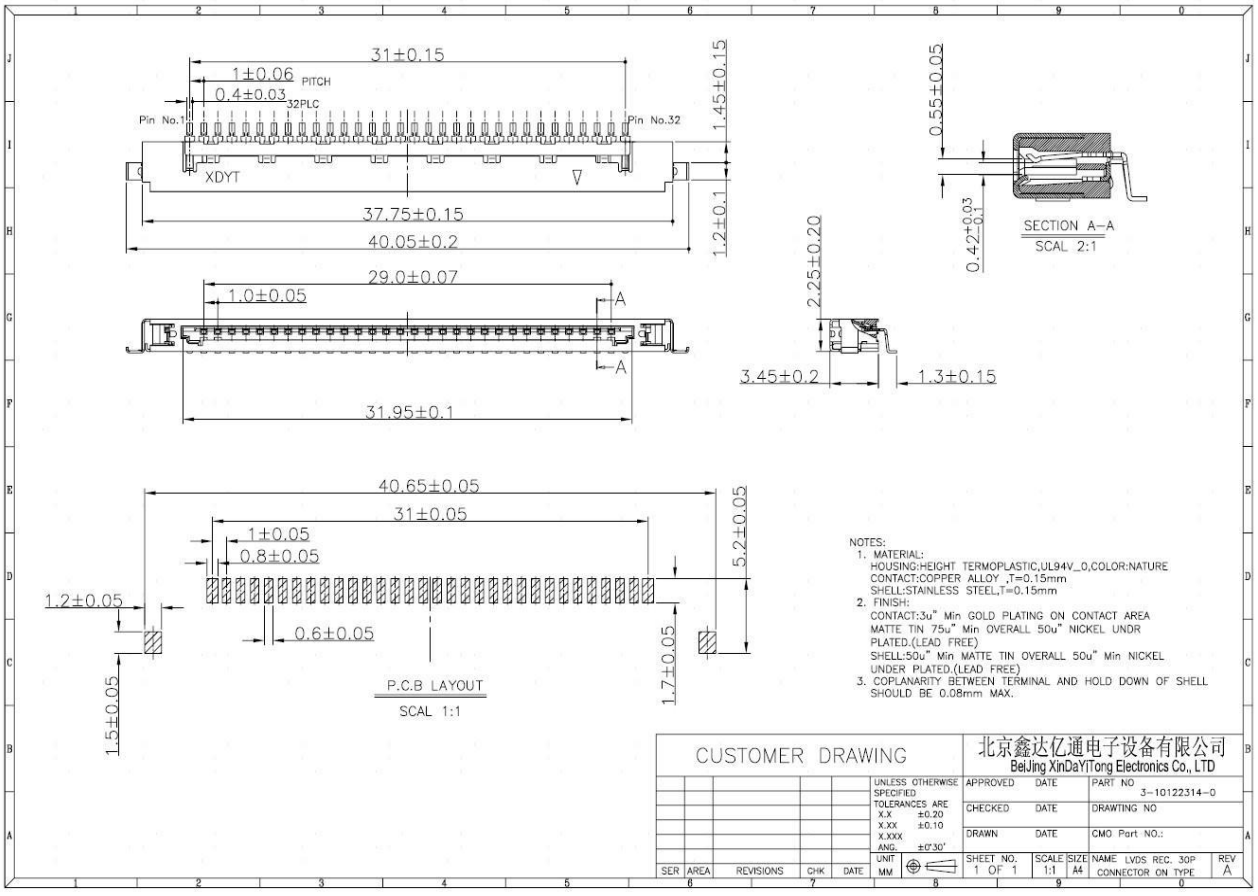


Fig. 3.5 LVDS connector direction sketch map

(2) For HKC used only, please leave it open.

Connector Drawing



4.2 Timing Spec.

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Clock	Frequency	F_{clkin}	50	74.25	90	MHz	(1)
	Input cycle to cycle jitter	Trcl	—	—	200	ps	(2)
	Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	—	Fclkin+2%	MHz	(3)
	Spread spectrum modulation frequency	FSSM	—	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	TRSM	-400	-	400	ps	(4)
Vertical Term	Frame Rate	**F**	48	60	76	Hz	
	Total	**T_V**	1094	1125	1836	T_H	$T_V = T_{VD} + T_{VB}$
	Active Display	**T_{VD}**	1080			T_H	
	Blank	**T_{VB}**	14	45	756	T_H	
Horizontal Term	Total	**T_H**	1050	1100	1678	T_{CLK}	$T_H = T_{HD} + T_{HB}$
	Active Display	**T_{HD}**	960			T_{CLK}	
	Blank	**T_{HB}**	90	140	718	T_{CLK}	

Note:

(1) Please make sure the range of pixel clock follows the following equations:

Fclkin(max) ≥Fmax × Tv×TH

Fmin × Tv ×TH ≥ Fclkin(min)

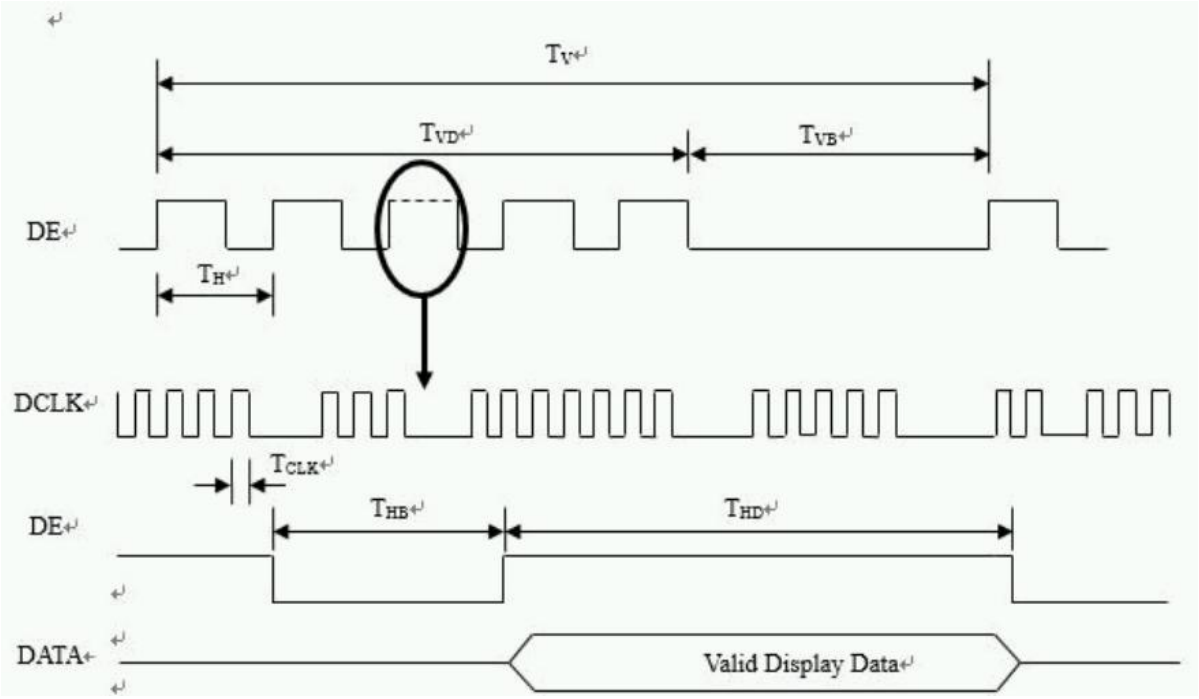


Fig 4.2 Signal timing diagram

(2)The input clock cycle-to-cycle is defined as below figures.

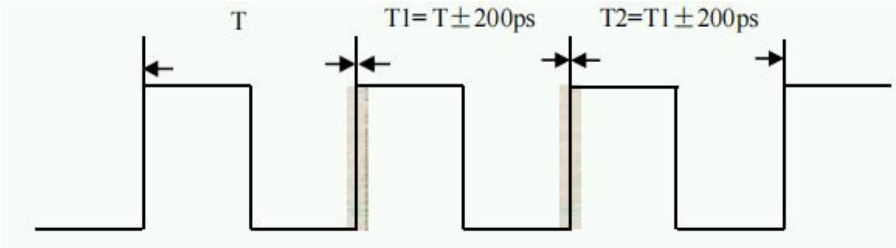


Fig 4.3 Jitter

(3) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure. The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM.

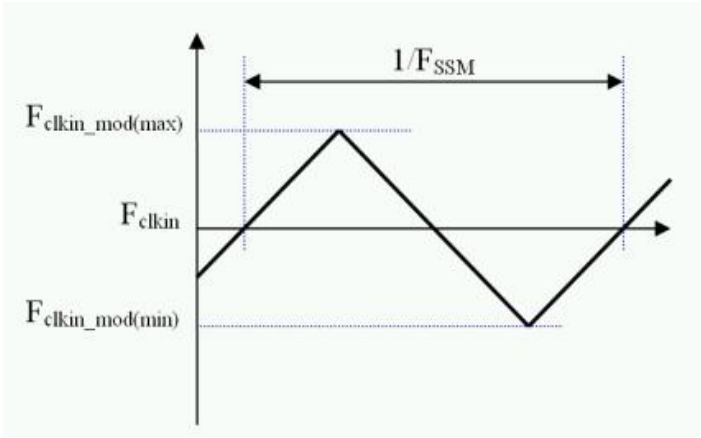


Fig 4.4 SSCG

(4) The LVDS timing diagram and setup/hold time is defined and showed as the following figure.

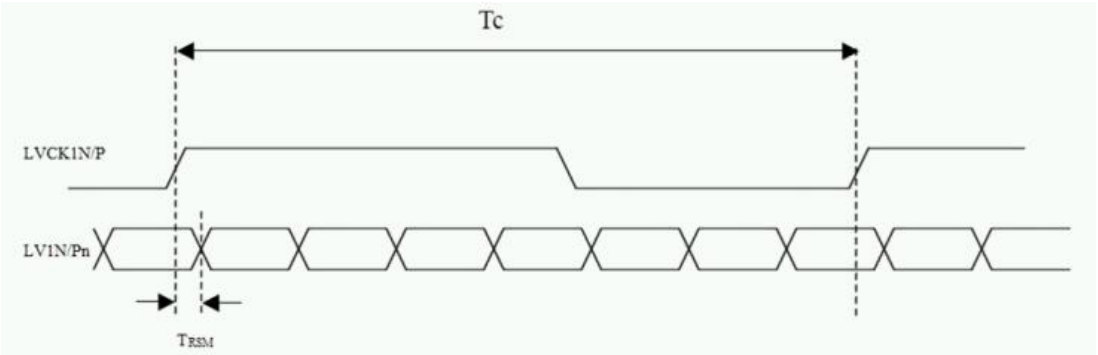


Fig 4.5 LVDS receive interface timing diagram

4.3 Backlight Electrical / Optical Characteristics

4.4.1 backlight connector

CN2 : PH 2.0 2P

Pin#	Signal Name
1	VDD＋ (Red)
2	VDD－(Black)

4.4.2 LED Bar

Parameter	Symbols	Min	Typ	Max	Unit
Forward Voltage (one circuit)	VF	2.8	-	3.2	MHz
Reverse Current (one circuit)	IR	-	-	10	μA
Forward Current	IF	-	90	120	Ma
Chromaticity Coordinates	X	0.268	0.279	0.285	
	Y	0.252	0.267	0.273	
Lumen	¢	20	22	24	LM
Viewing Angle	2θ1/2	-	120	-	Deg.
Number Of LED	Pcs	-	72	-	Pcs
Operation Voltage(LB)	VLB	50.4	-	57.6	V
Operation Current(LB)	ILB	-	240	-	mA
Power Consumption	PLB	12.096	-	13.824	W

5.0 POWER SEQUENCE

The power sequence specifications are shown as the following table and diagram

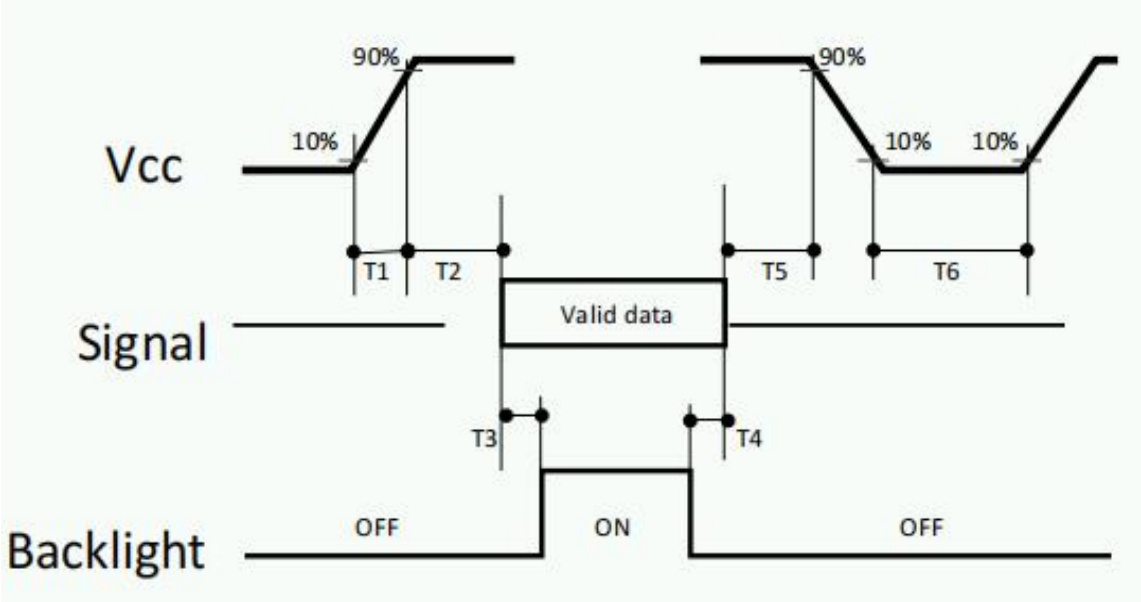


Fig5.0 Power on/off signal sequence

Parameter	Values			Unit
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	500	-	-	ms
T4	100	-	-	ms
T5	0	-	50	ms
T6	1000	-	-	ms

Attention:

(1)The supply voltage of the external system for the module input should be the same as the definition.

(2) To avoid some abnormal display noise, we suggest " VCC" falling time to follow "T6" definition.

(3) The product should be always operated within above ranges.

(4) In case of VCC is off level, please keep the level of input signals on the low or keep high impedance.

5.2 Flicker Adjustment

Flicker must be optimized after module assembly and aging. Its patterns are as follow:

sub pixel checker under 50% gray level.

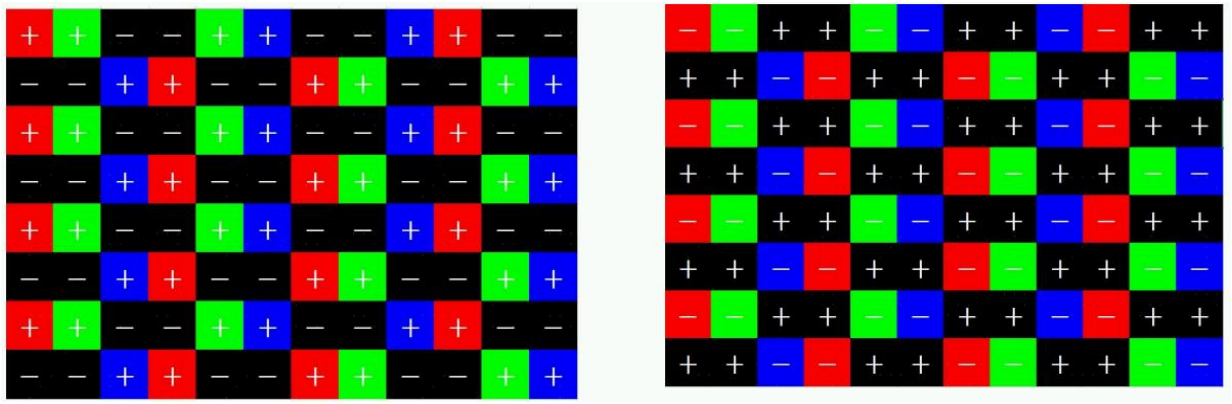


Fig5.2 Flicker pattern

5.3 Driver IC ESD Spec

If the LCD module is designed with the Plastic Bezel, we suggest ESD protection solutions should be applied to avoid IC damaged, as shown in Fig.3.12

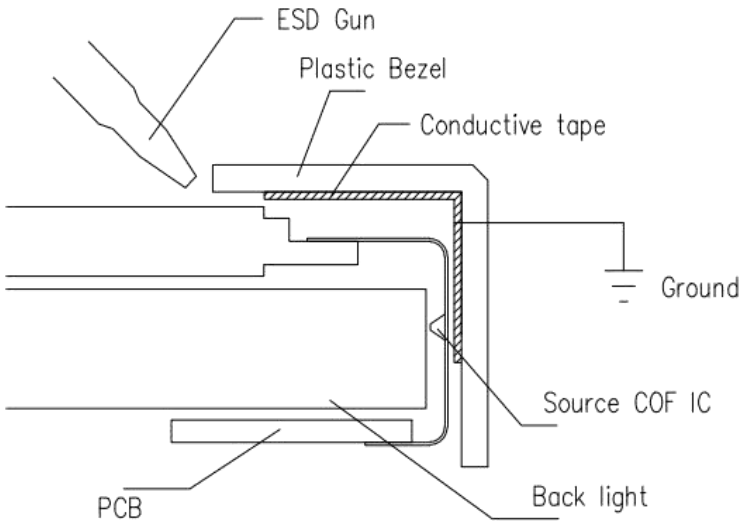


Fig5.3 Source COF IC ESD protection

6. Optical Specification

6.1 Test Condition

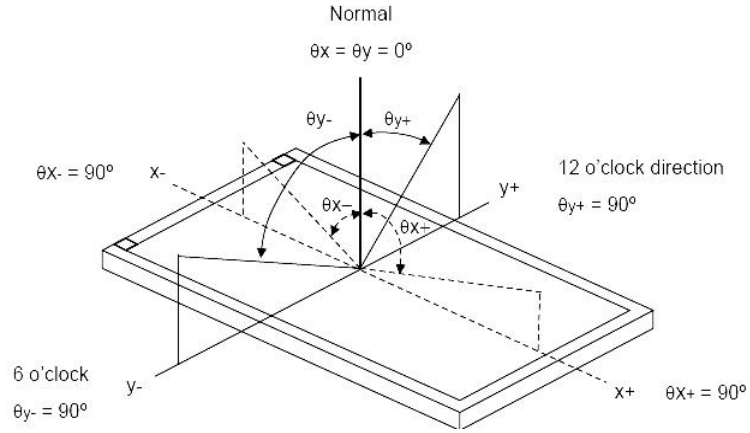
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25 ± 2	℃
Ambient Humidity	Ha	50 ± 10	%RH
Supply Voltage	Vcc	5.0	V
Input Signal	According to typical value in "3.Electrical characteristics		
LED Input Voltage	V_{LED}	51.5	V
LED Input Curent	I_{LED}	240.0	mA
Power Consumption	Pw	12.4	W

6.2 Optical Characteristics

The relative measurement methods of optical characteristics are shown as below.
The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (5).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0,θy=0, viewing normal angle	2000	3000	—	—	—
Response Time		Tr+Tf		—	7	—	ms	Note 3
Brightness unformity		BU		70	75	—	—	Note 2
Center Luminance of White		Lc		330	350	—	cd/m2	—
The color chromaticity	Red	Rx		Typ. -0.03	0.638	Typ. +0.03	—	—
		Ry			0.331		—	—
	Green	Gx			0.314		—	—
		Gy			0.617		—	—
	Blue	Bx			0.156		—	—
		By			0.143		—	—
	White	Wx			0.295		—	—
		Wy			0.335		—	—
Color Gamut		CG		68%	72%	—	—	Note 2
Viewing Angle	Horizental	θx+	CR≧10	75	89	—	Deg	Note 1
		θx-		75	89	—		
	Vertical	θy+		70	89	—		
		θy-		70	89	—		

Note 1: The definition of viewing angle



Note 2: Definition of luminance , CR measured positions and brightness uniformity

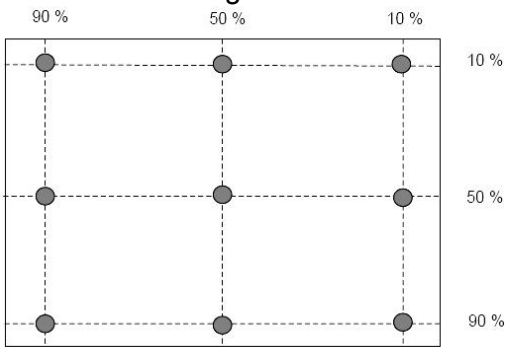
(a) Measure White luminance on the below 9 points and take the average value .

(b) CR : measures the same 9 points and take the average value .The Definition of Contrast Ratio is as folows :

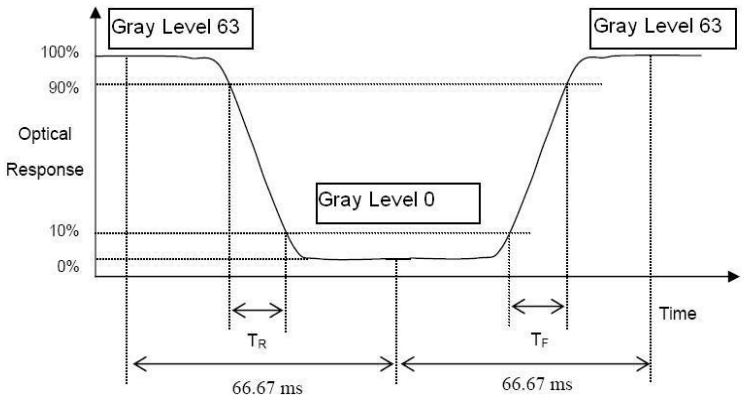
CR = ON(white L254)Luninance / OFF (Black L0)Luminance

(c) The definition of White Vibration

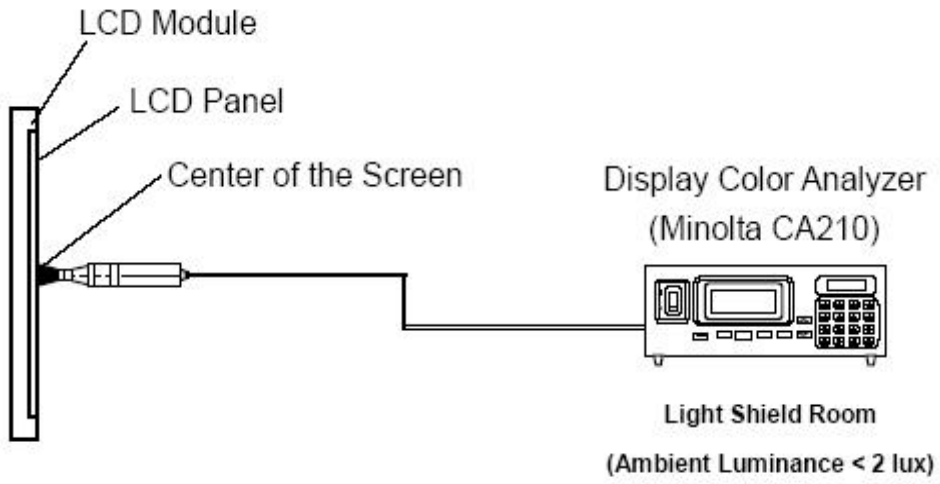
$$\frac{\text{The minimum brightness of 9 dot}}{\text{The maximum brightness of 9 dot}} \times 100\%$$



Note 3:Definition of Response Time (TR, TF):



Note 4: The measure method



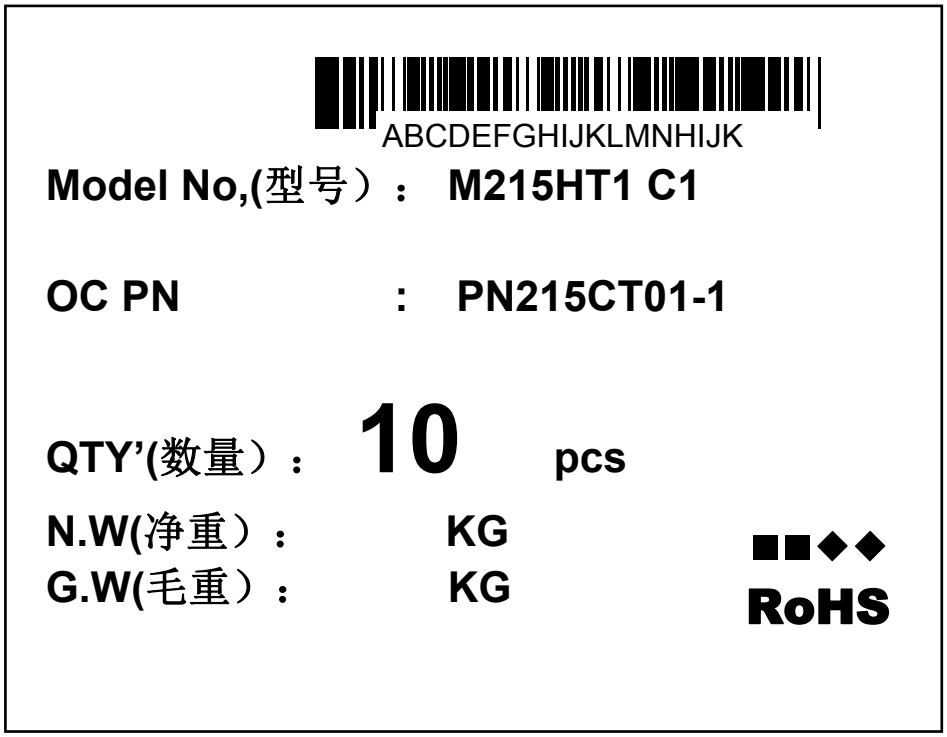
(a): The measurement point is the center of the active area except for the measurement of Luminance Uniformity

(b): Photometer :CA-210

7. Labels

7.1 Panel Label:

7.1 Carton Label:



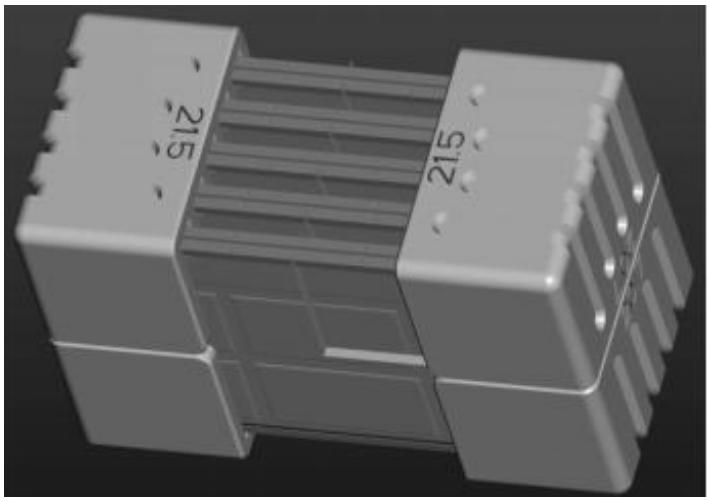
8. Packaging

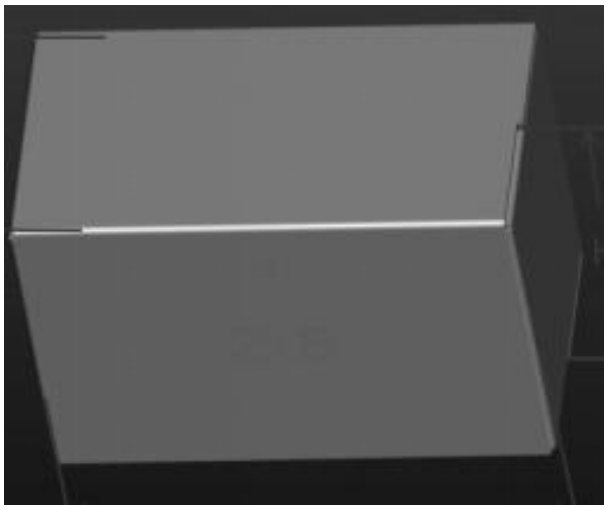
8.1 Carton(internal package)

(1)Packaging Form

(2) Packaging Method

(2) carton box size: 550*350*273mm





Note 1) Acceptable number of piling : 10 sets

8.2 Packing Mark

9. PRECAUTION

9.1 ASSEMBLY AND HANDLING PRECAUTIONS

1 Do not apply rough force such as bending or twisting to the module during assembly.
2 To assemble or install module into user's system can be in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
3 It's not permitted to have pressure or impulse on the module because the LED panel and Backlight will will be damaged.
4 Always follow the correct power sequence when LED module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
5 Do not pull the I/F connector in or out while the module is operating .
6 Do not disassemble the module.
Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very
7 soft and easily scratched.
8 It is dangerous that moisture come into or contacted the LED module, because moisture may damage LED module when it is operating.
9 High temperature or humidity may reduce the performance of module. Please store LED module within the specified storaged conditions.
10 When ambient temperature is lower than 10 ℃ may reduce the display quality. For example, the response time will become slowly.

7.2 SAFETY PRECAUTIONS

1 It is dangerous that moisture come into or contacted the LED module, because the moisture may damage LED module when it is operating.
2 If the liquid crystal material leaks from the panel,it should be kept away from the eyes or mouth, in case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
3 After the modlule's end of life, it is not harmful in case of normal operation and storage.

Outline dimension