PRODUCTION SPECIFICATION
OF TFT LCD MODULE

Model No. : M430C1B03 D3

OC PN: SG4251B03-3

CUSTOMER	
CONFIRMED BY	
APPROVED BY	

DILIANG ELECTRONICS	
PREPARED BY	
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Date	Rev.	Page	Old Description	New Description	Remark
2023.08.15	1.0	All	The specification was first issued		

1. GENERAL DESCRIPTION

1.1 OVERVIEW

The specification is applied to 32" module (M430C1B03 D3) used CSOT SG4251B03-3 opencell. This opencell is a diagonal 42.5" color active matrix LCD open cell with 2ch-LVDS interface. This open cell is a transmissive type display operating in the normally black mode. It supports 1920 * 1080 FHD resolution and can display up to 16.7M colors (8bit). Each pixel is divided into Red, Green and Blue sub-pixels which are arranged in vertical stripe. This open cell dedicates for LCD TV products and provides excellent performance which includes high brightness, ultra wide viewing angle, high color saturation and high color depth. CSOT open cell comply with RoHS for identification.

1.2 General Specifications

Item	Specification	Unit	Note
Active Area	940.896(H) × 529.254(V)	mm	
Module Size	**961.00(H) * 549.70 (V) * 17.10 (D)**	mm	
Module Weight	**8.80**	kg	Max.
Number of Pixels	1920 * 1080	pixel	
Pixel Pitch (Sub Pixel)	163.35(H) ×490.05(V)	um	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7 M	color	8bit
Display Mode	Normally Black		
Module Brightness	450(Min)	Cd/㎡	Typical value measured at DL BLU
Color Chroma	R = (0.643, 0.333)		
Contrast Ratio	G = (0.304, 0.601)		
	B = (0.139, 0.069)		
	W = (0.283, 0.297)		
	1200:1(Typ.)		
View Angle (CR 10)	+89/-89 (H), +89/-89 (V) (Typ.)		
Surface Treatment	Anti-glare, Haze 1%, Hard Coating (3H)		

1.3 Mechanical Specification

Item		Min	Typ	Max	Unit	Note
Weight		-500	**8300**	+500	g	-
Module Size	Horizontal(H)	(TYP)-1.0	**961.00**	(TYP)+1.0	mm	1
	Vertical (V)		**549.70**		mm	
	Depth(D)		**17.10**		mm	

2. Absolute Maximum Ratings

2.1 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[oC]	Note 3
Glass surface temperature (operation)	TGS	0	+65	[oC]	Note 3, Note 4
Operation Humidity	HOP	5	80	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[oC]	
Storage Humidity	HST	5	80	[%RH]	

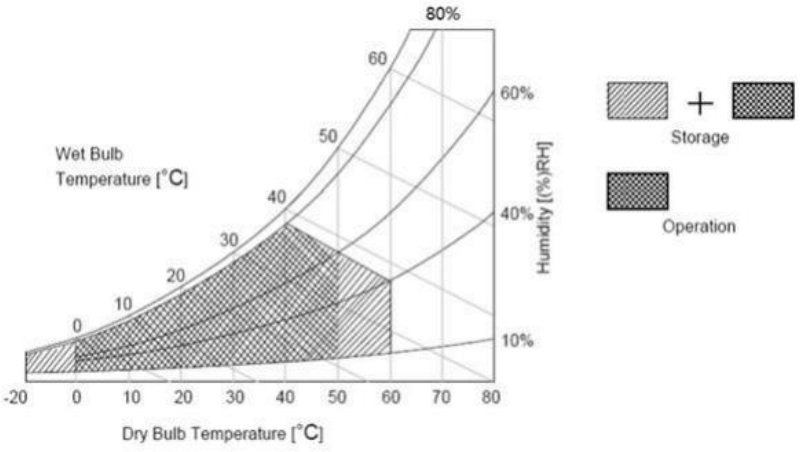
Note 1: With in Ta (25C)

Note 2: Permanent damage to the device may occur if exceeding maximum values.

Note 3: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max
2. Max wet-bulb temperature at 39

Note 4: Function Judged only



2.2 Backlight Unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LED operation Voltage	V_{led}	61.6	-	70.8	V_{led}	
LED operation Current	I_{led}	-	600	720	mA	- (1)
BackLight Power	P_{BL}	36.96	-	50.97	W	
Lift time	Lt	-	30000	-	Hrs	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal operating Conditions.

3. ELECTRICAL SPECIFICATIONS

3.1 Open Cell Electrical Specifications

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12.0	13.2	V	(1)
Rush Current		I_{RUSH}	-	-	3.00	A	(2)
Power Supply Current	White Pattern	I_{CC}	-	0.289	0.375	A	(3)
	Horizontal Stripe	I_{CC}	-	0.617	0.802	A	
	Black Pattern	I_{CC}	-	0.283	0.368	A	

Notes:

(1) The ripple voltage should be controlled less than 10% of VCC.

(2) Measurement condition: VCC = 12V, Rising time = 470 μ

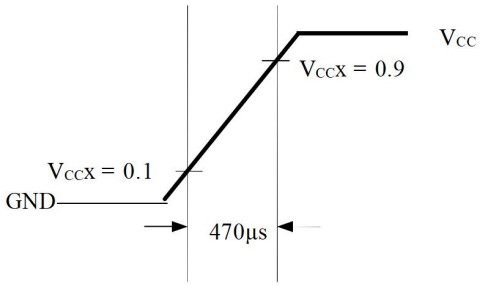


Fig. 3.1 VCC rising time condition

(3) Measurement condition: VCC = 12V, Ta = 25 ±2° C, F = 60 Hz. The test patterns are shown as below.

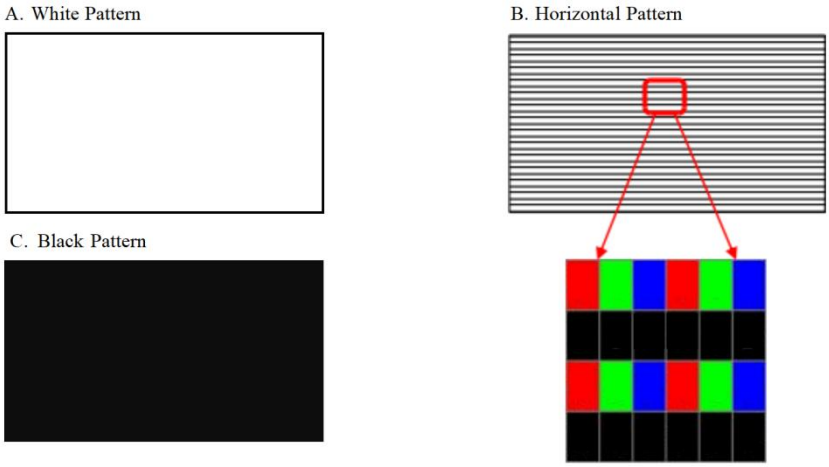


Fig. 3.2 Test patterns

3.2 LVDS Characteristics

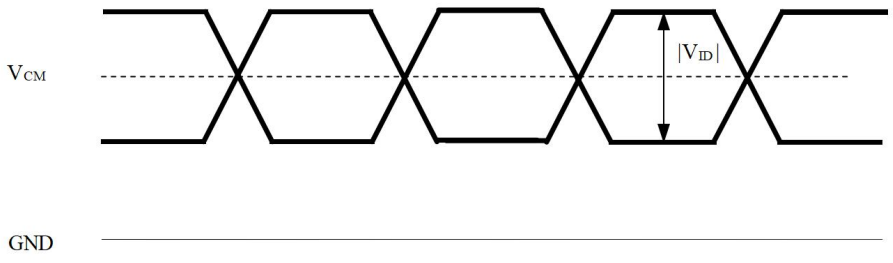
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
LVDS Interface	Differential Input High Threshold Voltage	V_{TH}	+100	-	-	mV	(1)
	Differential Input Low Threshold Voltage	V_{TL}	-	-	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential Input Voltage	$\|V_{ID}\|$	100	-	600	mV	
	Terminating Resistor	R_T	87.5	100	112.5	ohm	
CMOS Interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.7	V	

Note:

(1) This product should be always operated within above ranges.

(2) The LVDS input signal has been defined as follows:

Single and Signals



Differential Signal

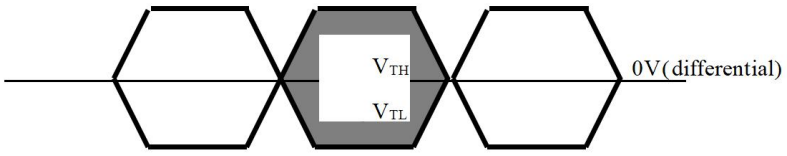


Fig. 3.3 LVDS input signal

3.3 Temperature Specifications

Parameter	Symbol	Spec			Unit	Note
		Min.	Typ.	Max.		
Source driver	Tc	-	-	115	℃	(1)
PMIC	Tc	-	-	100	℃	(1)
TCON	Tc	-	-	100	℃	(1)

Note:

(1) Any point on the IC surface must be less than Max. specification under any condition ,If the surface temperature is out of the specification, thermal solutions should be applied to avoid be damaged;

3.4 Driver IC ESD Specifications

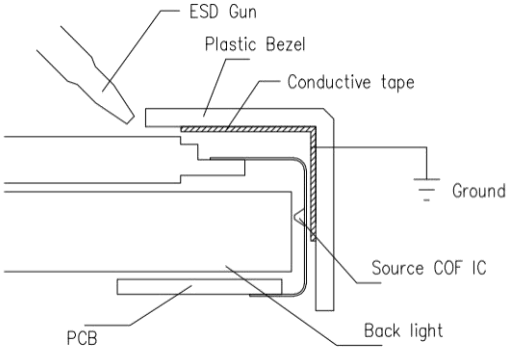


Fig. 3.4 Source COF IC ESD protection

3.5 Input Terminal Pin Assignment

3.5.1 Interface Pin Assignment

CN100: 187147-51221-3 (FCN) or equivalent (see Note (1))

Pin No.	Symbol	Description	Note
1	WP	Write Protect(Default:Low or Open ,High:Write Enable,Low or Open:Write Disable)	
2	SCL	I2C Serial Clock	
3	SDA	I2C Serial Data	
4	NC	No Connection	
5	NC	No Connection	
6	NC	No Connection	
7	LVDS_SEL	LVDS Data Format Selection(Default: Low VESA)	(2)
8	NC	No Connection	
9	NC	No Connection	
10	NC	No Connection	
11	GND	Ground	
12	RO[0]N	Odd LVDS Signal -	
13	RO[0]P	Odd LVDS Signal +	
14	RO[1]N	Odd LVDS Signal -	
15	RO[1]P	Odd LVDS Signal +	
16	RO[2]N	Odd LVDS Signal -	
17	RO[2]P	Odd LVDS Signal +	
18	GND	Ground	
19	ROCLK-	Odd LVDS Clock -	
20	ROCLK+	Odd LVDS Clock +	
21	GND	Ground	
22	RO[3]N	Odd LVDS Signal -	
23	RO[3]P	Odd LVDS Signal +	
24	NC	No Connection	
25	NC	No Connection	
26	NC	No Connection	
27	NC	No Connection	

28	RE[0]N	Even LVDS Signal -	
29	RE[0]P	Even LVDS Signal +	
30	RE[1]N	Even LVDS Signal -	
31	RE[1]P	Even LVDS Signal +	
32	RE[2]N	Even LVDS Signal -	
34	RE[2]P	Even LVDS Signal +	
34	GND	Ground	
35	RECLK-	Even LVDS Clock -	
36	RECLK+	Even LVDS Clock +	
37	GND	Ground	
38	RE[3]N	Even LVDS Signal -	
39	RE[3]P	Even LVDS Signal +	
40	NC	No Connection	
41	NC	No Connection	
42	NC	No Connection	
43	NC	No Connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	NC	No Connection	
48	12V	DC power supply	
49	12V	DC power supply	
50	12V	DC power supply	
51	12V	DC power supply	

Note:

(1)The direction of pin assignment is shown as below:

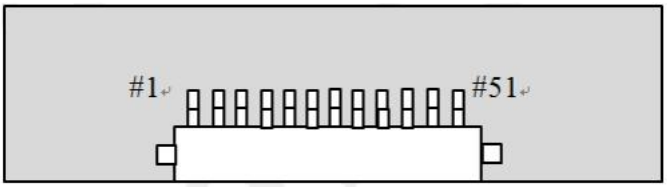


Fig. 3.5 Connector direction sketch map

(2) High: connect to + 3.3 V →JEIDA format; Low: connect to GND or Open →VESA format.

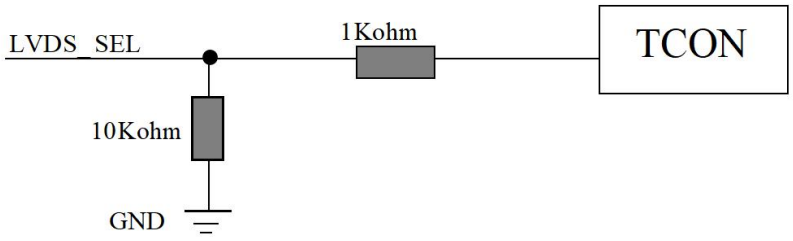


Fig. 3.6 LVDS_SEL PCBAset

3.6 Backlight Electrical / Optical Characteristics

3.6.1 backlight connector

"CN2 : PH2.0-2P

Pin#	Signal Name
1	VDD-
2	VDD+

"CN3 : PH2.0-2P

Pin#	Signal Name
1	VDD-
2	VDD+

3.6.2 LED Bar

Parameter	Symbols	Min	Typ	Max	Unit
Forward Voltage (one circuit)	VF	2.8	-	3.2	MHz
Reverse Current (one circuit)	IR	-	-	10	μA
Forward Current	IF	-	90	120	Ma
Chromaticity Coordinates	X	0.255	0.270	0.285	
	Y	0.225	0.240	0.255	
Lumen	¢	40	42	44	LM
Viewing Angle	2θ1/2	-	120	-	Deg.
Number Of LED	Pcs	-	176	-	Pcs
Operation Voltage(LB)	VLB	61.6	-	70.8	V
Operation Current(LB)	ILB	-	600	720	mA
Power Consumption	PLB	36.96	-	50.97	W

3.7 Block Diagram of Interface

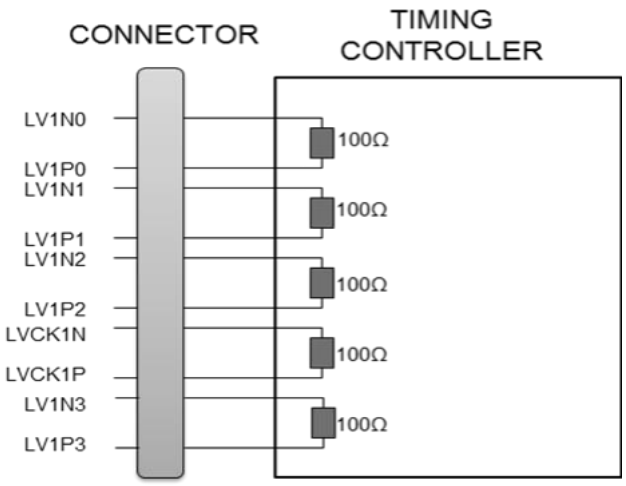


Fig. 3.7 Block diagram of interface

1. Attention:

(1) This open cell uses a 100 ohms (Ω) resistor between positive and negative lines of each receiver input.

(2) LVDS cable impedance shall be about 100 ohms per twist-pair line respectively

3.8 LVDS Interface

3.8.1 VESA Format (SELLVDS = L or Open)

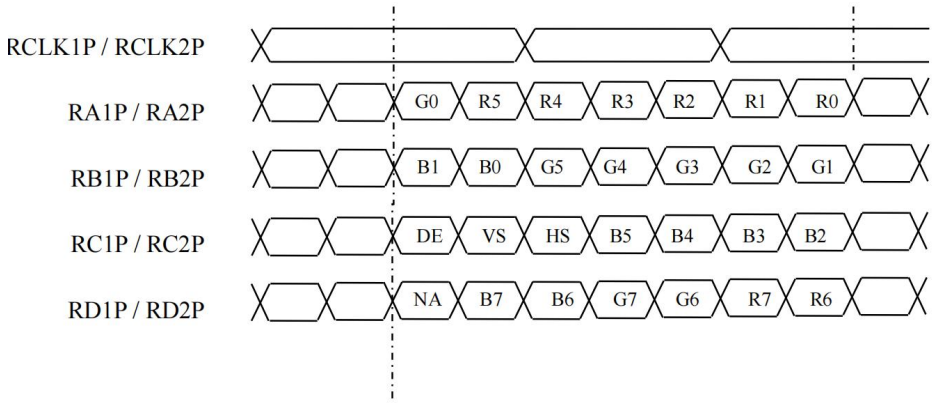


Fig. 3.8 VESA format

3.8.2 JEIDA Format (SELLVDS = H)

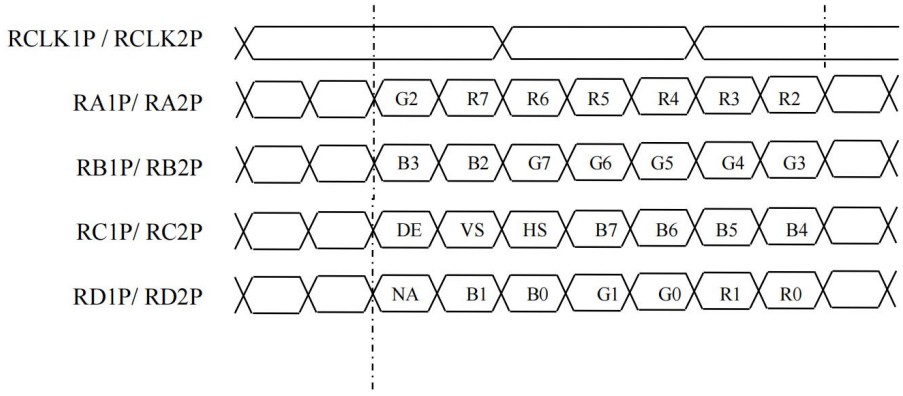
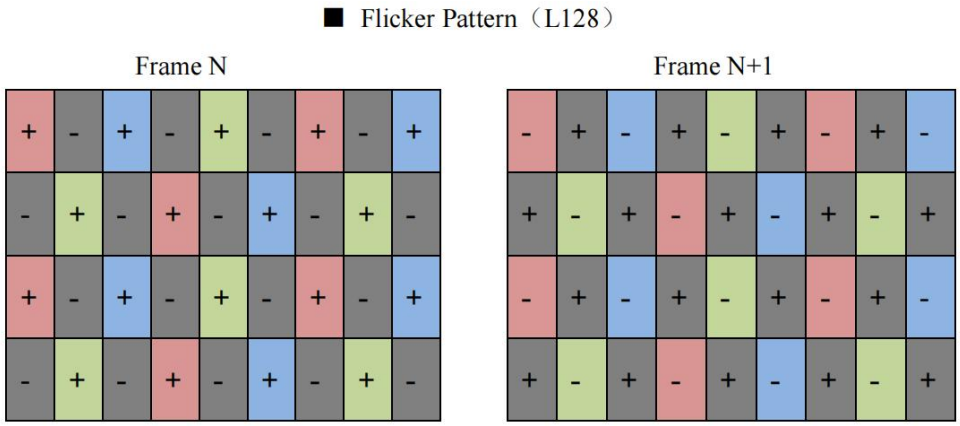


Fig. 3.9 JEIDA format

3.8.3 V-com Adjustment



3.9. Interface Timing

3.9.1 Timing Table (DE Only Mode)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	Fclkin (=1/T_{Clk})	65	74.25	80	MHz	(1) (2)
	Input cycle to cycle jitter	Trcl	-	-	200	ps	(3)
	Spread spectrum modulation range	Fclkin_mod	Fclkin-2%	-	Fclkin+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	0	-	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSM}	-400	-	400	ps	(5)
Vertical Active Display Term	Frame Rate	F	48	60	62.5	Hz	
	Total	T_V	1092	1125	1380	T_H	$T_V = T_{VD} + T_{VB}$
	Display	T_{VD}	1080			T_H	
	Blank	T_{VB}	12	45	300	T_H	
Horizontal Active Display Term	Total	T_H	1046	1100	1174	T_{CLK}	$T_H = T_{HD} + T_{HB}$
	Display	T_{HD}	960			T_{CLK}	
	Blank	T_{HB}	86	140	214	T_{CLK}	

Note:

(1) The TFT LCD open cell is operated in DE only mode, H sync and V sync input signal have no effect on normal operation.

(2) Please make sure the range of pixel clock follows the following equations:

Fclkin(max) ≥ F ×Tv ×Th F ×Tv ×Th ≥ Fclkin(min)

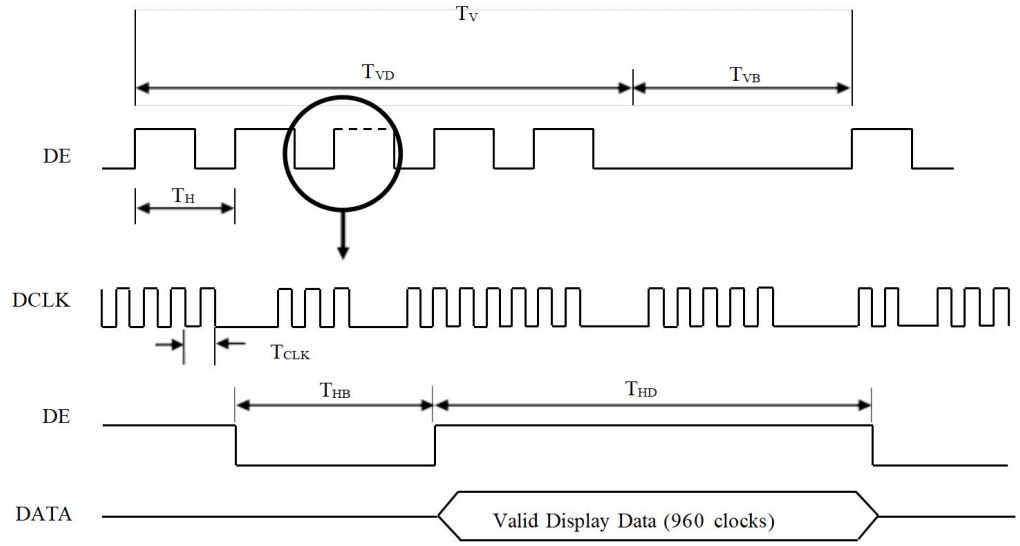


Fig. 3.10 Interface signal timing diagram

(3) The input clock cycle-to-cycle is defined as below figures.

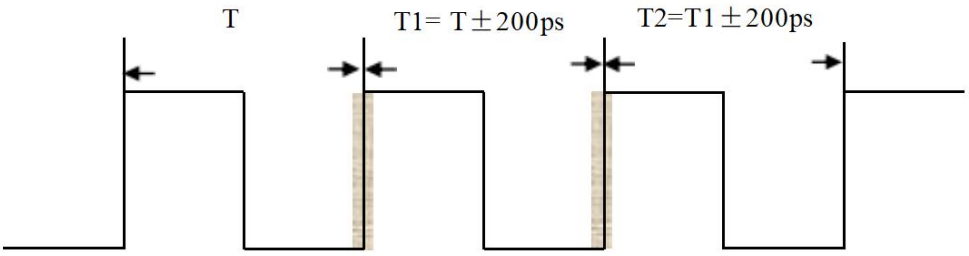


Fig. 3.11 Jitter

(4) The SSCG (Spread Spectrum Clock Generator) is defined as the following figure.

The LVDS SSM's suggestion is off by default, SOC board must test all validation if SOC board open the LVDS SSM.

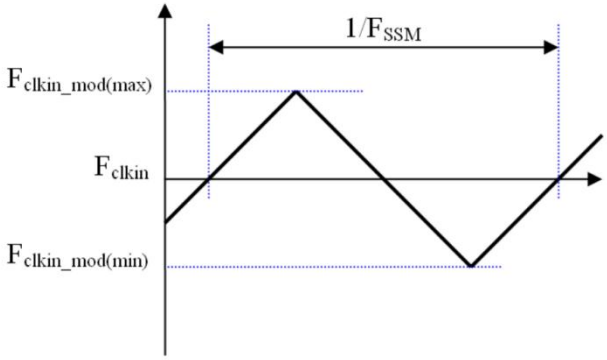


Fig. 3.12 SSCG

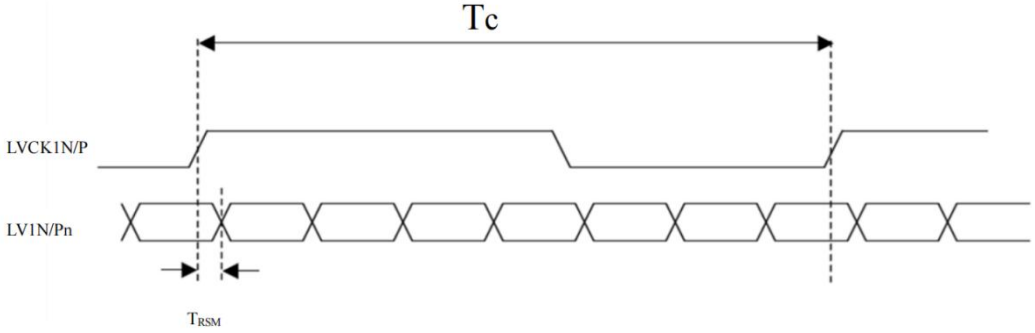


Fig.3.13 LVDS receive interface timing diagram

3.10 Power On/Off Sequence

To prevent a latch-up or DC operation of the Open cell, the power on/off sequence should be as the diagram below.

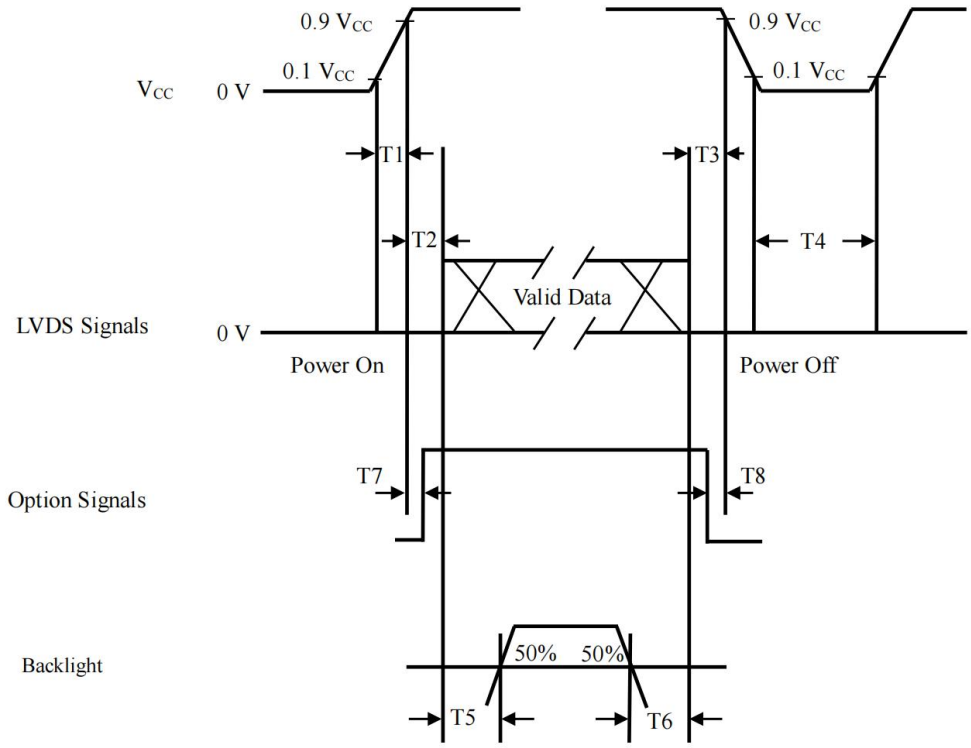


Fig.3.14 Power on/off sequence

Parameter	Values			Unit
	Min.	Typ.	Max.	Min.
T1	0.5	-	10.0	ms
T2	0.0	-	50	ms
T3	0.0	-	50	ms
T4	1000.0	-	-	ms
T5	500.0	-	-	ms
T6	100.0	-	-	ms
T7	-	-	T2	ms
T8	-	-	T3	ms

Attention:

(1) The supply voltage of the external system for the open cell input should follow the definition of VCC.

(2) When the customer's backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case that VCC is in off level, please keep the level of input signals on the low or high impedance. If T2 < 0, that may cause electrical overstress.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

4. Optical Characteristics

4.1 Test Condition

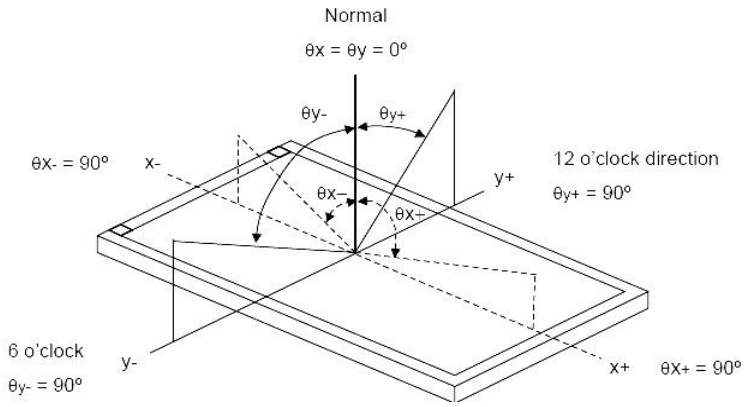
Item	Symbol	Value	Unit
Ambient Temperature	Ta	25 ± 2	℃
Ambient Humidity	Ha	50 ± 10	%RH
Supply Voltage	Vcc	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Input Voltage	V_{LED}	63.2	V
LED Input Current	I_{LED}	720	mA
Power Consumption	Pw	46.8	W

4.2 Optical Characteristics

The relative measurement methods of optical characteristics are shown as below.
The following items should be measured under the test conditions described in 4.1

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0,θy=0, viewing normal angle	—	4000	—	—	—
Response Time		TL		—	6.5	12	ms	Note 3
Brightness uniformity		BU		70	75	—	—	Note 2
Center Luminance of White		Lc		400	450	—	cd/m2	—
The color chromatic	Red	Rx		Typ. -0.03	0.643	Typ. +0.03	—	—
		Ry			0.333		—	—
	Green	Gx			0.304		—	—
		Gy			0.601		—	—
	Blue	Bx			0.136		—	—
		By			0.069		—	—
	White	Wx			0.283		—	—
		Wy			0.297		—	—
	Color Gamut	CG		—	72	—	—	—
Viewing Angle	Horizontal	θx+	CR≧10	—	89	—	Deg	Note 1
		θx-		—	89	—		
	Vertical	θy+		—	89	—		
		θy-		—	89	—		

Note 1: The definition of viewing angle



Note 2: Definition of luminance , CR measured positions and brightness uniformity

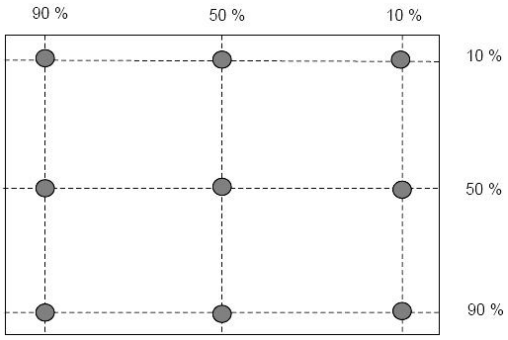
(a) Measure White luminance on the below 9 points and take the average value .

(b) CR : measures the same 9 points and take the average value .The Definition of Contrast Ratio is as follows :

CR = ON(white L255)Luminance / OFF (Black L0)Luminance

(c) The definition of White Vibration

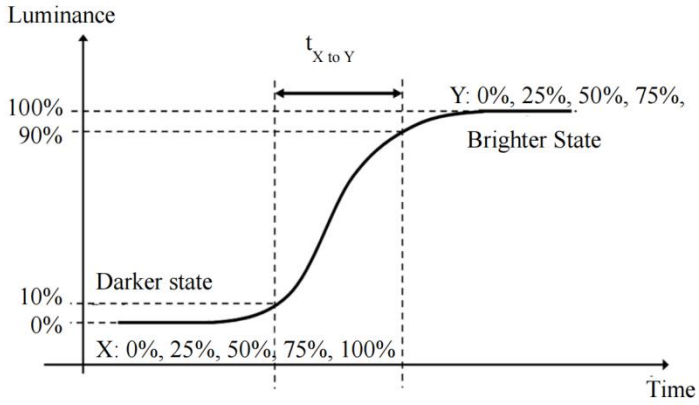
$$\frac{\text{The minimum brightness of 9 dot}}{\text{The maximum brightness of 9 dot}} \times 100\%$$



Note 3:Response time TL is defined as the average transition time in the response time matrix. The table below is the response time matrix in which each element tX to Y is the transition time from luminance ratio X to Y. X and Y are two different luminance ratios among 0%, 25%, 50%, 75%, and 100% luminance. The transition time tX to Y is defined as the time taken from 10% to 90% of the luminance difference between X and Y (X < Y) as illustrated in Fig.6.4. When X > Y, the definition of tX to Y is the time taken from 90% to 10% of the luminance difference between X and Y. The response time is optimized on refresh rate Fr = 60Hz.

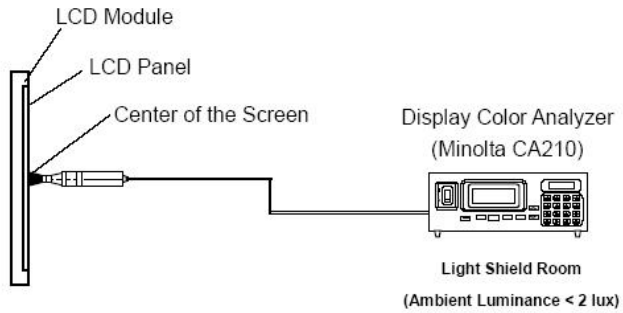
Measured Transition Time						
		0%	25%	50%	75%	100%
Luminance Ratio of Current Frame	0%		$t_{25\% \text{ to } 0\%}$	$t_{50\% \text{ to } 0\%}$	$t_{75\% \text{ to } 0\%}$	$t_{100\% \text{ to } 0\%}$
	25%	$t_{0\% \text{ to } 25\%}$		$t_{50\% \text{ to } 25\%}$	$t_{75\% \text{ to } 25\%}$	$t_{100\% \text{ to } 25\%}$
	50%	$t_{0\% \text{ to } 50\%}$	$t_{25\% \text{ to } 50\%}$		$t_{75\% \text{ to } 50\%}$	$t_{100\% \text{ to } 50\%}$
	75%	$t_{0\% \text{ to } 75\%}$	$t_{25\% \text{ to } 75\%}$	$t_{50\% \text{ to } 75\%}$		$t_{100\% \text{ to } 75\%}$
	100%	$t_{0\% \text{ to } 100\%}$	$t_{25\% \text{ to } 100\%}$	$t_{50\% \text{ to } 100\%}$	$t_{75\% \text{ to } 100\%}$	

tX to Y means the transition time from luminance ratio X to Y.



All the transition time is measured at the center point of the LCD module by ELDIM OPTI Scope-SA.

Note 4: The measure method



(a) : The measurement point is the center of the active area except for the measurement of Luminance Uniformity

(b) : Photometer :CA-210

5.0 Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50℃， 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50℃， 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0℃， 300hours	
High Temperature Storage (HTS)	Ta= 60℃， 300hours	
Low Temperature Storage (LTS)	Ta= -20℃， 300hours	
Thermal Shock Test (TST)	-20℃/30min, 60℃/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (Electro Static Discharge)	Contact Discharge: ± 4KV, 150pF(330) 1sec, 8 points, 25 times/ point. Air Discharge: ± 8KV, 150pF(330) 1sec 8 points, 25 times/ point.	2

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: EN61000-4-2, ESD class B: Certain performance degradation allowed

No data lost

Self-recoverable

No hardware failures.

6.0 Shipping Label

6.1Panel Label

6.2 Carton Label

7. Packaging

9.1 Carton(internal package)

(1)Packaging Form

(2) Packaging Method

(3) Carton box size : 1025*310*640mm

(4) Gloss weight of 1 carton: 34.60KG

(5) Packing pictures :

Note 1) Acceptable number of piling : 4 sets

7.2 Packing Mark

8. PRECAUTION

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

1 Do not apply rough force such as bending or twisting to the module during assembly.
2 To assemble or install module into user's system can be in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
3 It's not permitted to have pressure or impulse on the module because the LED panel and Backlight will will be damaged.
4 Always follow the correct power sequence when LED module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
5 Do not pull the I/F connector in or out while the module is operating .
6 Do not disassemble the module.
Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very
7 soft and easily scratched.
8 It is dangerous that moisture come into or contacted the LED module, because moisture may damage LED module when it is operating.
9 High temperature or humidity may reduce the performance of module. Please store LED module within the specified storage conditions.
10 When ambient temperature is lower than 10 ℃ may reduce the display quality. For example, the response time will become slowly.

8.2 SAFETY PRECAUTIONS

1 It is dangerous that moisture come into or contacted the LED module, because the moisture may damage LED module when it is operating.
2 If the liquid crystal material leaks from the panel,it should be kept away from the eyes or mouth, in case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
3 After the modlule's end of life, it is not harmful in case of normal operation and storage.

9. Outline dimensions