

	PRODUCTION SPECIFICATION OF TFT LCD MODULE	Model No: M430BF91 C1
		OC PN: HV430FHB-F91

+

**PRODUCTION SPECIFICATION
OF TFT LCD MODULE**

Model No. : M430BF91 C1

OC PN: HV430FHB-F91

CUSTOMER	
CONFIRMED BY	
APPROVED BY	

DILIANG ELECTRONICS	
PREPARED BY	
CONFIRMED BY	



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Date	Rev.	Page	Old Description	New Description	Remark
2023.08.15	1.0	All	The specification was first issued		
2023.10.13	1.1	3	Module Size: 961.00(H) * 549.70 (V) * 17.10 (D)	Module Size: 963.20(H) * 556.80 (V) * 19.20 (D)	New Structure Up date
		26	Module Weight: 8.80 Outline dimensions	Module Weight: 8.80 Outline dimensions	



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1. GENERAL DESCRIPTION

1.1 OVERVIEW

The specification is applied to 32" module (M430BF91 C1) used BOE HV430FHB-F91 opencell. This opencell is a color active matrix TFT LCD open cell using amorphous silicon TFT'S (Thin Film Transistors) as an active switching devices. This module has a 43 inch diagonally measured active area with FHB resolutions (1920 horizontal by 1080 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in Z- inversion stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.

1.2 Features

- .Mini-LVDS interface with 2 ports 3 pairs
- .High-speed response
- .Low color shift image quality
- .8-bit color depth, display 16.7M colors
- .High luminance and contrast ratio, low reflection and wide viewing angle
- .Gate driver use GOA mode
- .ADS technology is applied for high display quality
- . RoHS compliant

1.3 General Specifications

Item	Specification	Unit	Note
Active Area	940.896(H) × 529.254(V)	mm	
Module Size	963.20(H) * 556.80 (V) * 19.20 (D)	mm	
Module Weight	8.60	kg	Max.
Number of Pixels	1920 * 1080	pixel	
Pixel Pitch (Sub Pixel)	163.35(H) × 490.05(V)	um	
Pixel Arrangement	RGB Vertical Stripe	-	
Display Colors	16.7 M	color	8bit
Display Mode	Normally Black		
Module Brightness	450(Min)	Cd/m ²	Typical value measured at DL BLU
Color Chroma	R = (0.648, 0.322)		
Contrast Ratio	G = (0.285, 0.629)		
	B = (0.152, 0.049)		
	W = (0.283, 0.297)		
	1200:1(Typ.)		
View Angle (CR 10)	+89/-89 (H), +89/-89 (V) (Typ.)		
Surface Treatment	Anti-glare, Haze 1%, Hard Coating (3H)		

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1.4 Mechanical Specification

Item		Min	Typ	Max	Unit	Note
Weight		-1000	8600	+1000	g	-
Module Size	Horizontal(H)	(TYP)-1	963.20	(TYP)+1	mm	1
	Vertical (V)		556.80		mm	
	Depth(D)		19.20		mm	



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2. Absolute Maximum Ratings

2.1 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[oC]	Note 3
Glass surface temperature (operation)	TGS	0	+65	[oC]	Note 3, Note 4
Operation Humidity	HOP	5	80	[%RH]	Note 3
Storage Temperature	TST	-20	+60	[oC]	
Storage Humidity	HST	5	80	[%RH]	

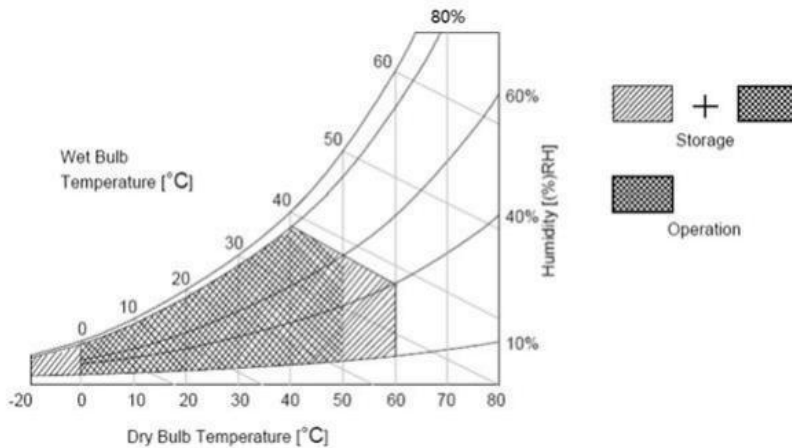
Note 1: With in Ta (25C)

Note 2: Permanent damage to the device may occur if exceeding maximum values.

Note 3: Temperature and relative humidity range are shown as the below figure.

1. 90% RH Max
2. Max wet-bulb temperature at 39

Note 4: Function Judged only



2.2 Backlight Unit

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
LED operation Voltage	V_{led}	61.6	-	70.8	V_{led}	
LED operation Current	I_{led}	-	600	720	mA	(1)
BackLight Power	P_{BL}	-	-	50.97	W	
Lift time	Lt	-	30000	-	Hrs	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal operating Conditions.

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3. ELECTRICAL SPECIFICATIONS

3.1 Open Cell Electrical Specifications

Characteristics	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	VSS	-8.1	-8	-7.9	V
DC Supply Voltage	LVSS	-10.2	-10	-9.8	V
DC Supply Voltage	VGH	33.5	34	34.5	V
DC Supply Voltage	DVDD3V3	3.25	3.3	3.4	V
DC Supply Voltage	VCOM0	6.46	6.51	6.56	V
DC Supply Voltage	HAVDD	7.19	7.24	7.29	V
DC Supply Voltage	AVDDS	14.96	15.06	15.16	V
DC Supply Voltage	GMA1	14.03	14.08	14.13	V
DC Supply Voltage	GMA4	11.47	11.52	11.57	V
DC Supply Voltage	GMA5	10.69	10.74	10.79	V
DC Supply Voltage	GMA6	9.98	10.03	10.08	V
DC Supply Voltage	GMA9	7.74	7.79	7.84	V
DC Supply Voltage	GMA10	6.64	6.69	6.74	V
DC Supply Voltage	GMA13	4.4	4.45	4.5	V
DC Supply Voltage	GMA14	3.69	3.74	3.79	V
DC Supply Voltage	GMA15	2.91	2.96	3.01	V
DC Supply Voltage	GMA18	0.36	0.41	0.46	V

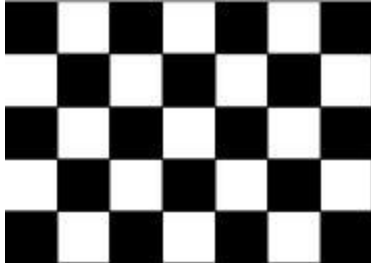
Notes:

1. VTERM: For CML Mode only, LVDS Mode keeps NC. LVDS Mode S-IC logic power needs 1.8V only, CML Mode S-IC logic power needs 1.8V and VTERM needs 1.2V.
2. VGH should be tested on SOC board or separate power board. High voltage of STV/CLK/VDDODD/VDDEVEN is as same as VGH voltage.
3. Other test points are on source board. Use typical pattern to test.

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3.2 Power Consumption and Flicker Pattern

a) Typ : Mosaic 7X5 (L0/L255)



b) Max : Sub Horizontal 1 Line (L0/L255)



c) Flicker Test Pattern



3.3 Driver Characteristics

Parameter	Symbol	Values			Unit	Remark
		Min	Typ	Max		
Driver Surface Temperature	T _{DS}	-	-	125	°C	Note1

Note 1. Any point on the driver surface must be less than 125 °C under any conditions.

2. This test condition is based on BOE module.

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3.1 Interface Pin Assignment

3.2.1 Connector Pin Configuration

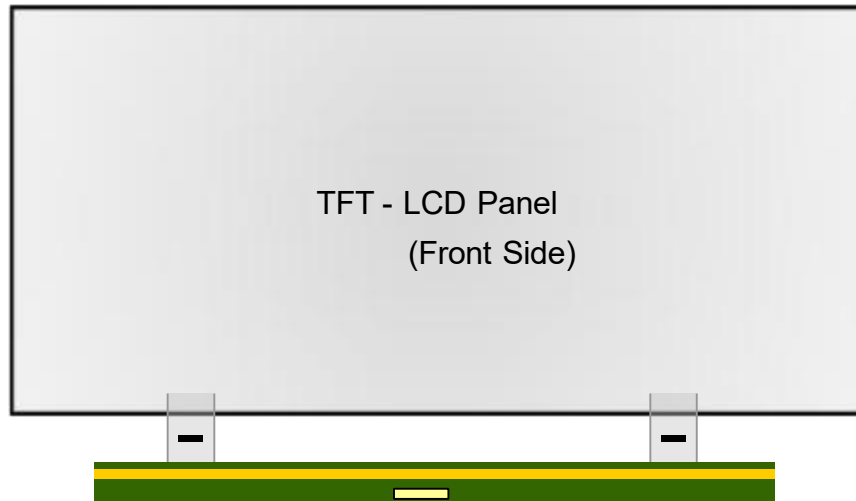
<Open Cell XPCB Input Connector Pin Configuration >

Pin No	Symbol	Description	Pin No	Symbol	Description
1	GND	Ground	35	GND	Ground
2	STV0	STV Signal for GOA	36	LML_0N	mini-LVDS signal
3	STV1	STV Signal for GOA	37	LML_0P	mini-LVDS signal
4	CLK1	CLOCK Signal for GOA	38	LML_1N	mini-LVDS signal
5	CLK2	CLOCK Signal for GOA	39	LML_1P	mini-LVDS signal
6	CLK3	CLOCK Signal for GOA	40	LML_2N	mini-LVDS signal
7	CLK4	CLOCK Signal for GOA	41	LML_2P	mini-LVDS signal
8	CLK5	CLOCK Signal for GOA	42	GND	Ground
9	CLK6	CLOCK Signal for GOA	43	LML_CKN	mini-LVDS signal Clock
10	CLK7	CLOCK Signal for GOA	44	LML_CKP	mini-LVDS signal Clock
11	CLK8	CLOCK Signal for GOA	45	GND	Ground
12	NC	Not Connected	46	RML_0N	mini-LVDS signal
13	VDD1	VDD Signal for GOA	47	RML_0P	mini-LVDS signal
14	NC	Not Connected	48	RML_1N	mini-LVDS signal
15	VDD2	VDD Signal for GOA	49	RML_1P	mini-LVDS signal
16	NC	Not Connected	50	RML_2N	mini-LVDS signal
17	VSS	Negative Power Supply	51	RML_2P	mini-LVDS signal
18	LVSS	Low Negative Power Supply	52	GND	Ground
19	GND	Ground	53	RML_CKN	mini-LVDS signal Clock
20	NC	Not Connected	54	RML_CKP	mini-LVDS signal Clock
21	TP	Source driver latch signal	55	GND	Ground
22	POL1	Source driver polarity inversion signal	56	DVDD	Power Supply +3.3V
23	POL2	Source driver polarity inversion signal	57	DVDD	Power Supply +3.3V
24	GND	Ground	58	GND	Ground
25	GAM18	Gamma Reference Voltage	59	AVDDS	AVDD Power Supply
26	GAM15	Gamma Reference Voltage	60	AVDDS	AVDD Power Supply
27	GAM14	Gamma Reference Voltage	61	AVDDS	AVDD Power Supply
28	GAM13	Gamma Reference Voltage	62	AVDDS	AVDD Power Supply
29	GAM10	Gamma Reference Voltage	63	NC	Not Connected
30	GAM9	Gamma Reference Voltage	64	HAVDD	Half AVDD Power Supply
31	GAM6	Gamma Reference Voltage	65	HAVDD	Half AVDD Power Supply
32	GAM5	Gamma Reference Voltage	66	VCOM0	Panel Common Electrode
33	GAM4	Gamma Reference Voltage	67	VCOM0	Panel Common Electrode
34	GAM1	Gamma Reference Voltage	68	GND	Ground

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Notes :

1. NC (Not Connected) : These pins show status of T/con board and are only used for BOE internal operations.
2. XPCBL and XPCBR Input pins assignments refer to the below diagram.



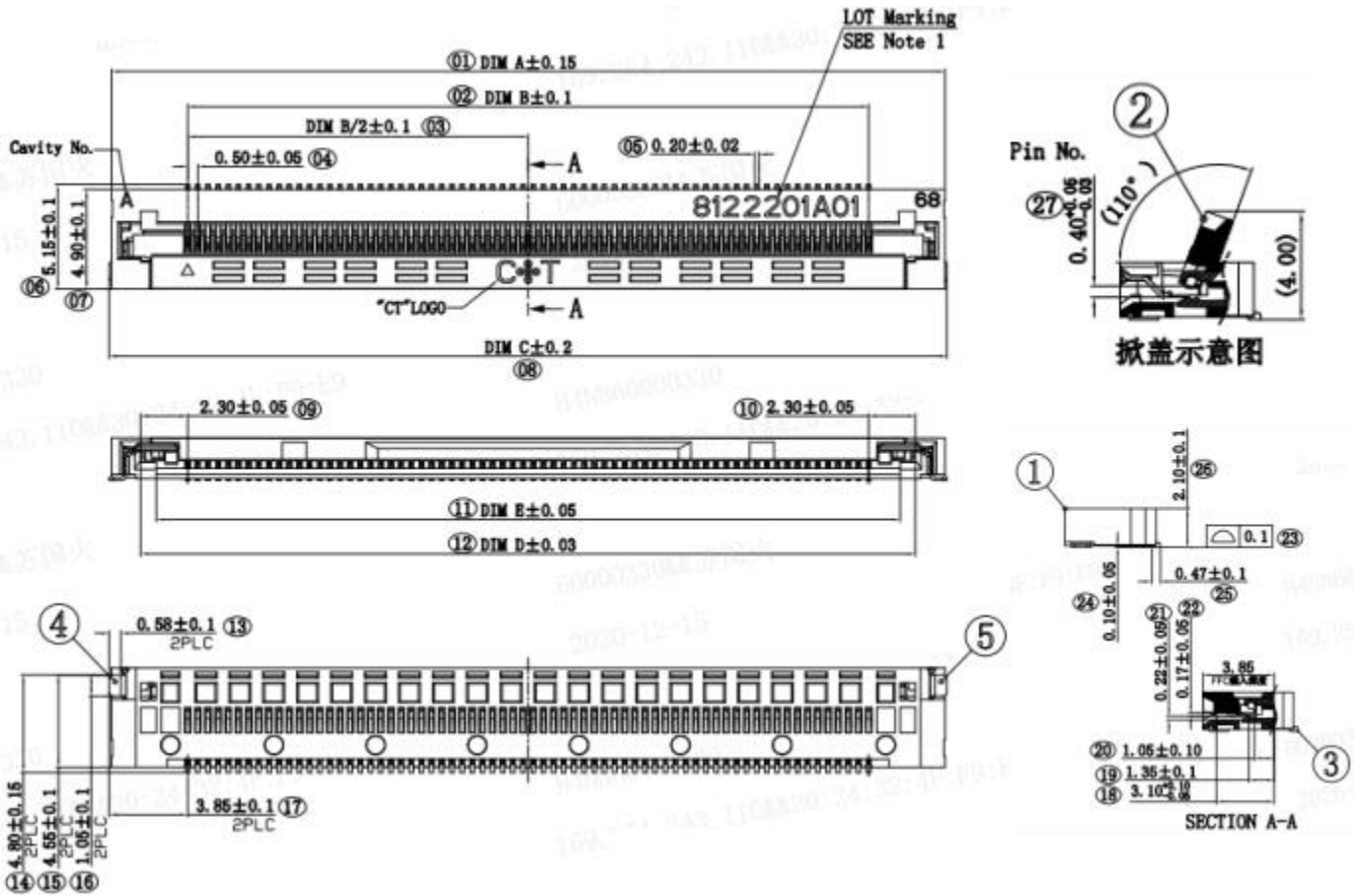
3. GAM2/GAM3/GAM7/GAM8/GAM11/GAM12/GAM16/GAM17 should be disconnected on SOC board. If these pins are connected, 0V is prohibited.
4. SHL should keep high voltage (+3.3V) after control IC initialized.
5. PAIR should keep low voltage (0V) after control IC initialized.
6. VCOM0 is DC power supply for panel common electrode.

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3.2.2 Open Cell Input Connector & FFC Drawing

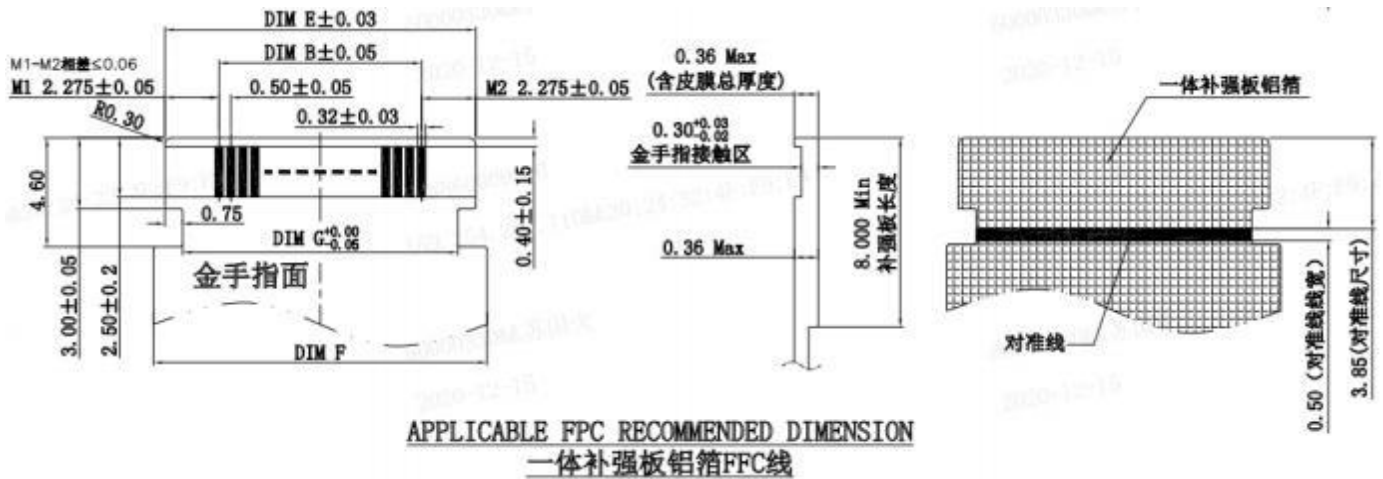
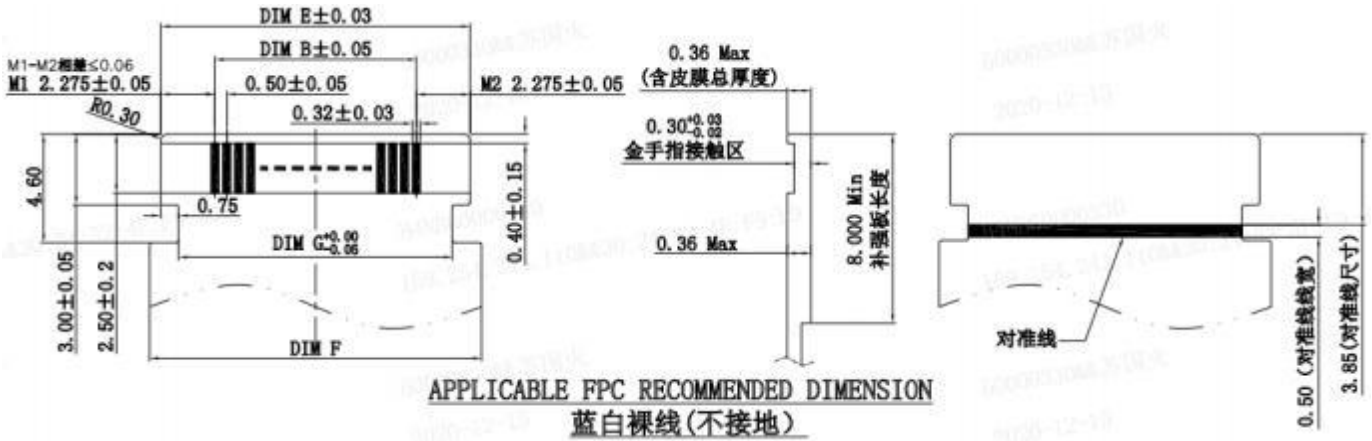


PIN NO.	DIM A	DIM B	DIM C	DIM D	DIM E
68	41.00	33.50	41.20	38.10	36.6

Note: XPCB board input connector is the same as T/con board output connector.

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68pin Connector Drawing-PM.FPC.LVS4906801



PIN NO.	DIM B	DIM E	DIM F	DIM G
68	33.50	38.05	39.00	36.55

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3.3 Backlight Electrical / Optical Characteristics

3.3.1 backlight connector

"CN2 : PH2.0-2P

Pin#	Signal Name
1	VDD-
2	VDD+

"CN3 : PH2.0-2P

Pin#	Signal Name
1	VDD-
2	VDD+

3.3.2 LED Bar

Parameter	Symbols	Min	Typ	Max	Unit
Forward Voltage (one circuit)	VF	2.8	-	3.2	MHz
Reverse Current (one circuit)	IR	-	-	10	μA
Forward Current	IF	-	90	120	Ma
Chromaticity Coordinates	X	0.255	0.270	0.285	
	Y	0.225	0.240	0.255	
Lumen	ℓ	40	42	44	LM
Viewing Angle	2θ1/2	-	120	-	Deg.
Number Of LED	Pcs	-	176	-	Pcs
Operation Voltage(LB)	VLB	61.6	-	70.8	V
Operation Current(LB)	ILB	-	600	720	mA
Power Consumption	PLB	36.96	-	50.97	W



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3.4. Timing spec

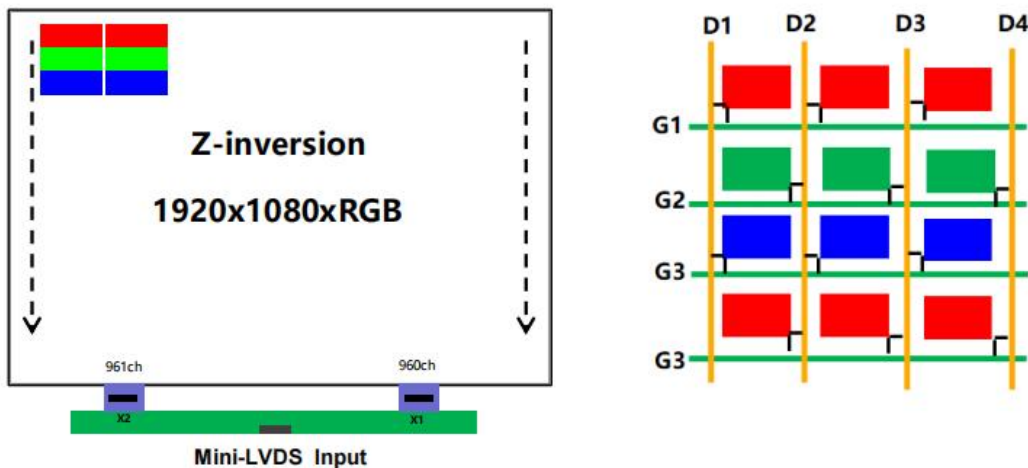
3.4.1 Timing Parameters

Item	Symbols	Min	Typ	Max	Unit	
Pixel Clock Frequency	1/Tc	69	74.25	77	MHz	
Frame Rate	F	47	60(50)	63	Hz	
Vertical	Total	T _V	1085	1125(1350)	1380	T _H
	Display	T _{VD}	1080			T _H
	Blank	T _{VB}	50	70(270)	300	T _H
Horizontal	Total	T _H	1050	1100	1647	T _{CLK}
	Display	T _{HD}	960			T _{CLK}
	Blank	T _{HB}	90	140	687	T _{CLK}

Notes:

- 1.This product is DE only mode. The input of Hsync & Vsync signal does not have an effect on normal operation.
2. This product should keep clock frequency and Horizontal value fixed when adjusting frame rate.
3. It is recommended that the PWM frequency should be an integer multiple of the frame rate , If BLU use PWM mode.

3.4.2 Pixel Structure



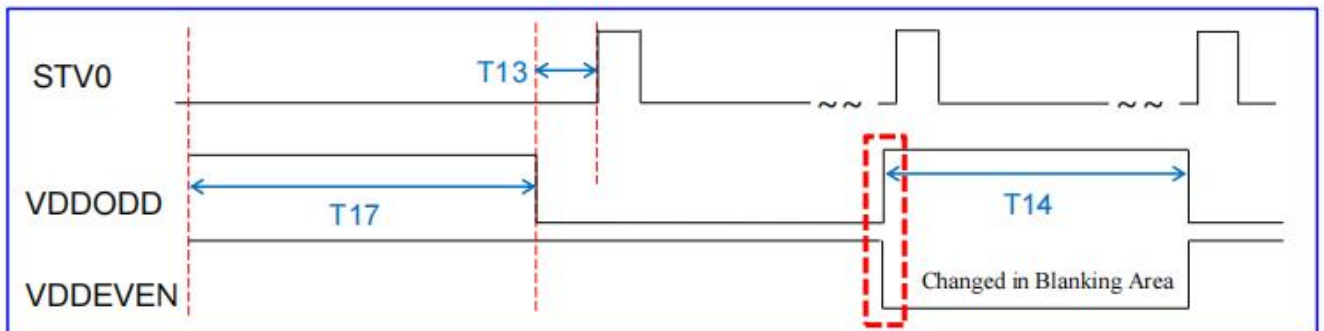
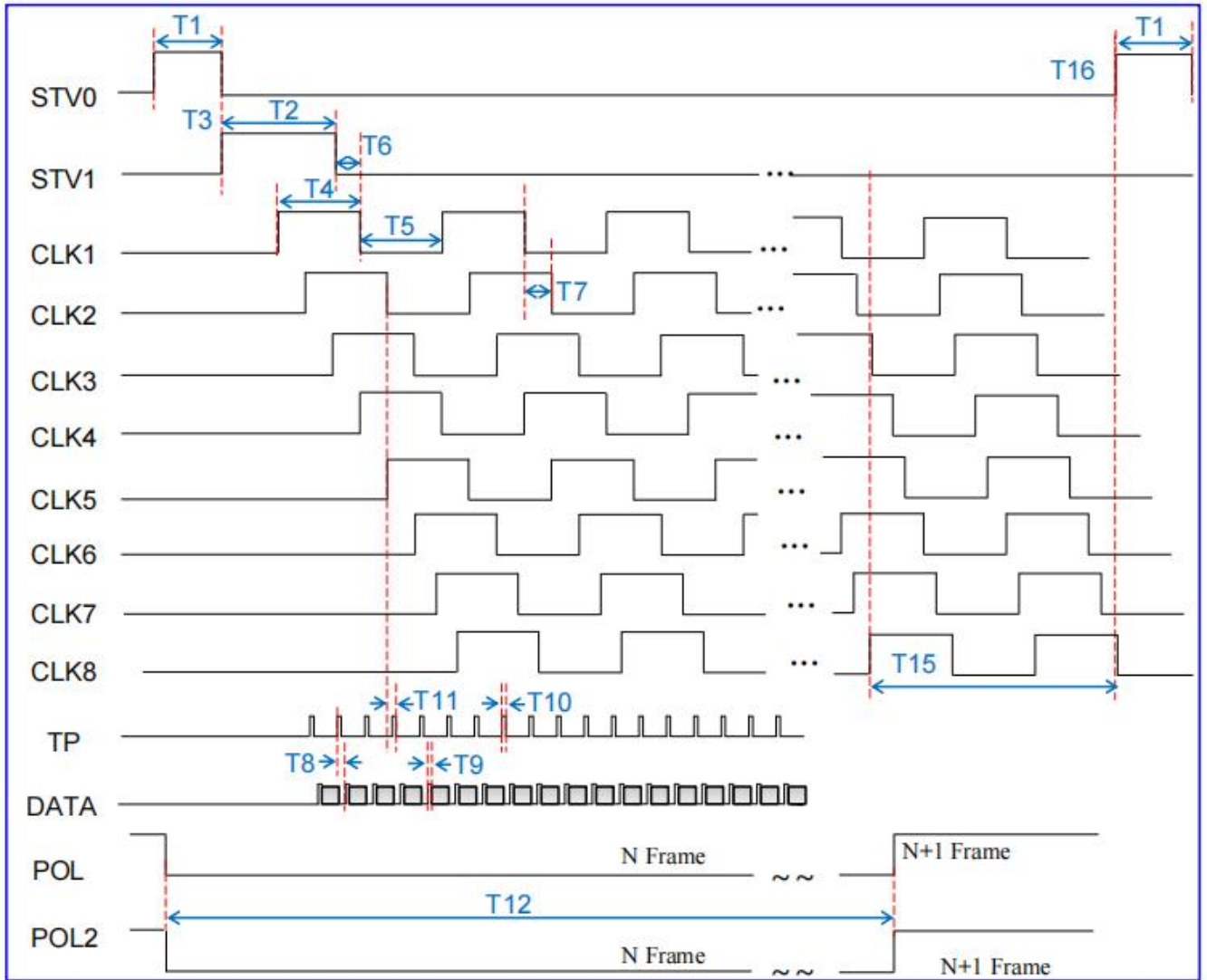
Notes:

1. Panel is progressive scan from top to bottom.
2. Source driver data latch direction is from left to right.

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3.4.3 Signal Timing Waveform

H total :2200
V total :1125
Frame Rate:60Hz



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H total :2200

V total :1125

Frame Rate:60Hz

Parameter	Min.	Typ.	Max.		Remark
T1	-	14.8us	-	STV0 Width(3H)	
T2	-	29.6us	-	STV1 Width(6H)	
T3	-	0	-	STV0 Falling to STV1 Rising	
T4	-	14.8us	-	CLK1 High Width(3H)	Note1
T5	-	24.7us	-	CLK1 Low Width(5H)	Note2
T6	-	4.94us	-	STV1 Falling to CLK1 Falling	
T7	-	4.94us	-	CLK1 Falling to CLK2 Falling	Note3
T8	-	400ns	-	TP Rising to Reset Rising	
T9	-	76ns	-	Reset Width	
T10	-	250ns	-	TP Width	
T11	-	1.4us	-	CLK Edge to TP Falling(GOE)	
T12	-	16.67ms	-	POL and POL2 Width	
T13	-	33.3ms	-	VDD1 and VDD2 Power On Timing	
T14	-	2s	-	VDD1 and VDD2 width	
T15	-	16H(2 Period)	-	Dummy CLK Period	
T16	-	0	-	Dummy CLK Falling To STV0 Rising	
T17	-	50ms	-	VDDO/E Keep Same Phase Period	

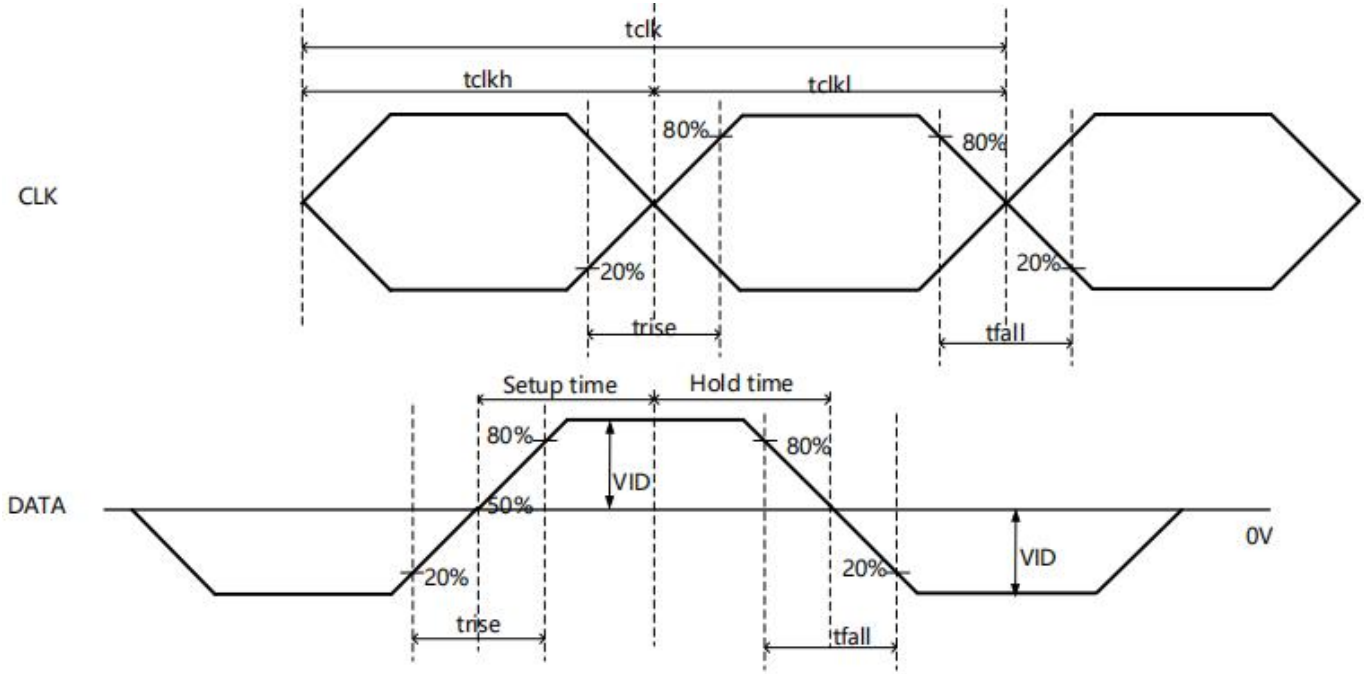
Notes:

1. CLK2~CLK8 High Width is T4, same as CLK1.
2. CLK2~CLK8 Low Width is T5, same as CLK1.
3. CLK2 Falling to CLK3 Falling, CLK3 Falling to CLK4 Falling, CLK4 Falling to CLK5 Falling, CLK5 Falling to CLK6 Falling, CLK6 Falling to CLK7 Falling, CLK7 Falling to CLK8 Falling are all T5.
4. When power on, STV and CLK1~CLK8 should keep low before the first STV.
5. STV and CLK1~CLK8 should keep low in vertical blanking time.
6. POL1 and POL2 must reverse in vertical blanking time.
7. VDD1 and VDD2 must reverse in vertical blanking time.



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3.5 Signal Eye Diagram



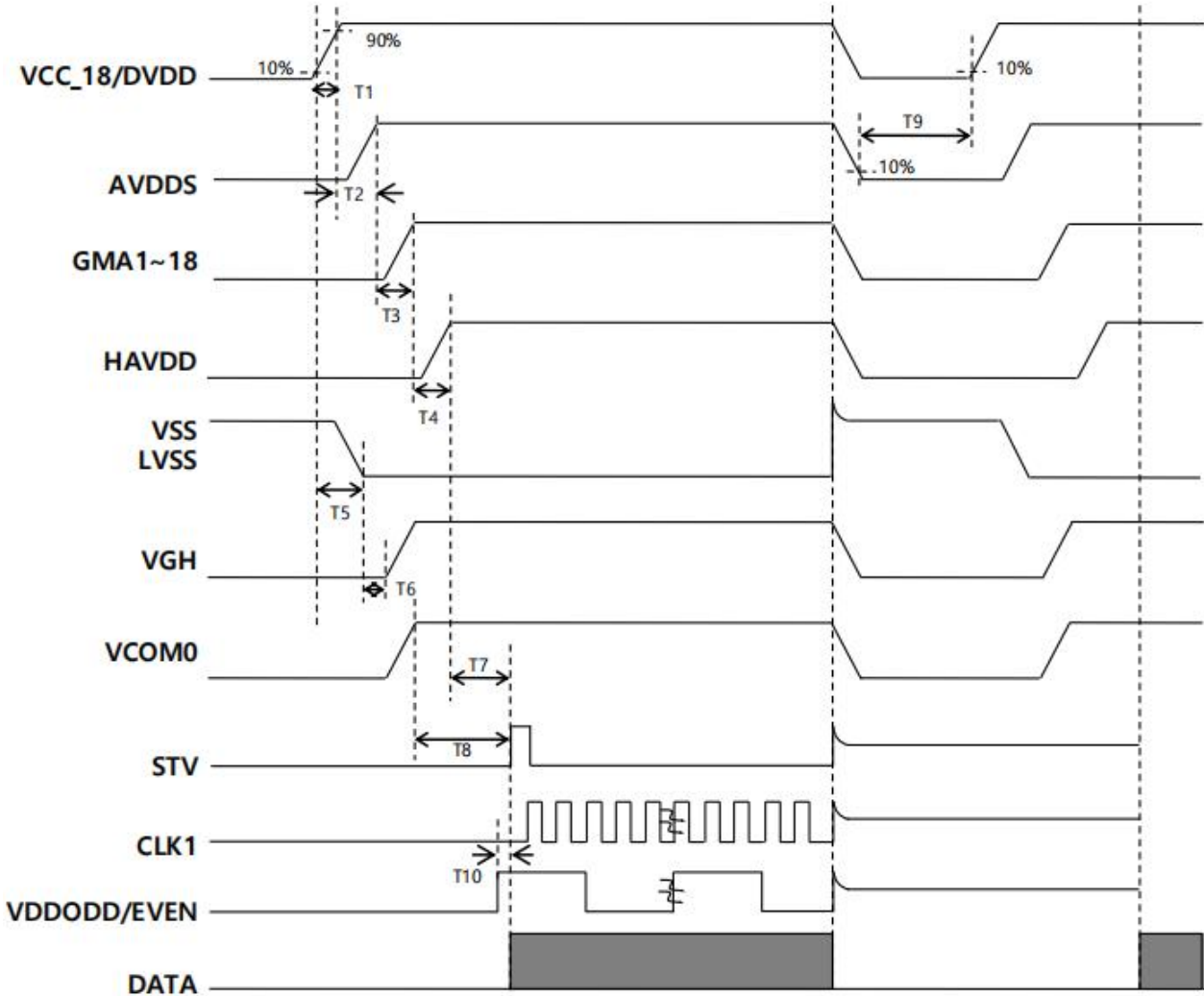
Parameter	Symbol	Spec			Unit
		Min	Typ	Max	
Clock Period	t_{clk}	2.5	-	-	ns
Clock low pulse width	t_{clkh}	$0.4t_{clk}$	-	$0.6t_{clk}$	ns
Clock high pulse width	t_{clkl}	$0.4t_{clk}$	-	$0.6t_{clk}$	ns
Data setup time	t_{setup}	0.6	-	-	ns
Data hold time	t_{hold}	0.6	-	-	ns
CLK,Data rising time	t_{rise}	-	-	0.4	ns
CLK,Data falling time	t_{fall}	-	-	0.4	ns
mini-LVDS different voltage	VID	120	-	-	mv

- Notes :
1. Eye diagram test point is located on source board, close to source driver.
 2. Condition: Mini-LVDS CLK MAX Frequency ≤ 250 Mhz.



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3.6 POWER SEQUENCE



Notes :

1. When power off, VGL(VSS),STV,CLK,VDDODD/VDDEVEN timing should follow VGH falling.
2. VGH is on SOC board or separate power board only, so T6 time is tested on SOC board or separate power board.



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T	Min	Type	Max	Unit	Note
T1	0	-	10	ms	
T2	0	-	-	ms	
T3	0	-	-	ms	AVDDS must be higher than HAVDD and GMA all the time
T4	-T3	-	1000	ms	AVDDS must be higher than HAVDD and GMA all the time
T5	0	-	-	ms	
T6	0	-	-	ms	
T7	0	-	-	ms	
T8	0	-	-	ms	
T9	1	-	-	s	
T10	50	-	-	ms	VDD should pull high before 1 st STV rising



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4. Optical Characteristics

4.1 Test Condition

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25 ± 2	°C
Ambient Humidity	Ha	50 ± 10	%RH
Supply Voltage	Vcc	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Input Voltage	V _{LED}	63.2	V
LED Input Current	I _{LED}	600	mA
Power Consumption	Pw	37.90	W

4.2 Optical Characteristics

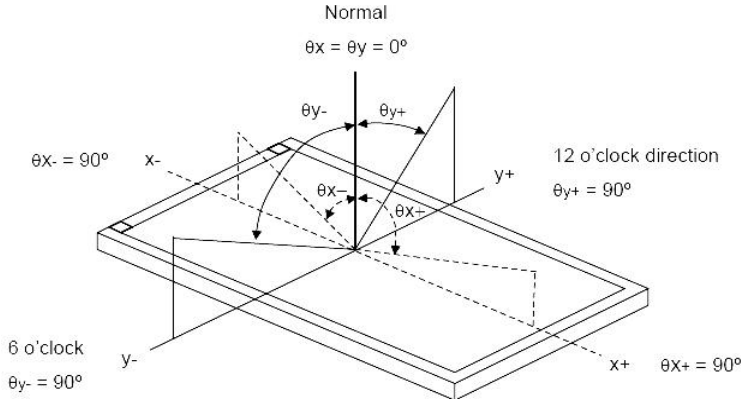
The relative measurement methods of optical characteristics are shown as below.

The following items should be measured under the test conditions described in 4.1

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio	CR	θ _x =0,θ _y =0 , viewing normal angle	—	1200	—	—	—	
Response Time	TL		—	8	10	ms	Note 3	
Brightness uniformity	BU		70	75	—	—	Note 2	
Center Luminance of White	L _c		400	450	—	cd/m ²	—	
The color chromatic	Red		R _x	Typ. -0.03	0.640	Typ. +0.03	—	—
			R _y		0.327		—	—
	Green		G _x		0.313		—	—
			G _y		0.590		—	—
	Blue		B _x		0.139		—	—
			B _y		0.070		—	—
	White	W _x	0.283		—		—	
W _y		0.297	—	—				
Viewing Angle	Horizontal	θ _{x+}	CR ≧ 10	—	89	—	Deg	Note 1
		θ _{x-}		—	89	—		
	Vertical	θ _{y+}		—	89	—		
		θ _{y-}		—	89	—		

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Note 1: The definition of viewing angle



Note 2: Definition of luminance , CR measured positions and brightness uniformity

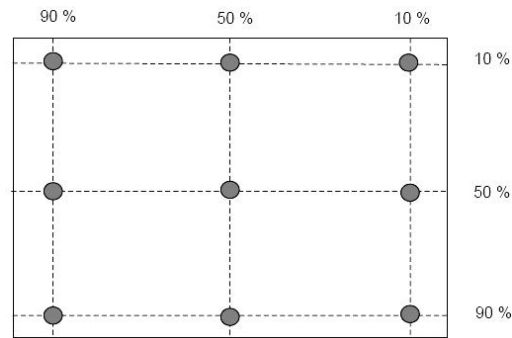
(a) Measure White luminance on the below 9 points and take the average value .

(b) CR : measures the same 9 points and take the average value .The Definition of Contrast Ratio is as follows :

$$CR = \frac{ON(\text{white L63})\text{Luminance}}{OFF(\text{Black L0})\text{Luminance}}$$

(c) The definition of White Vibration

$$\frac{\text{The minimum brightness of 9 dot}}{\text{The maximum brightness of 9 dot}} \times 100\%$$



Note 3:Response time Tg is the average time required for display transition by switching the input signal as below table and is based on Frame rate fV = 60Hz with BOE Tcon Board to optimize. Each time in below table shall be measured by switching the input signal for “any level of gray(bright)”and “any level of gray(dark)”



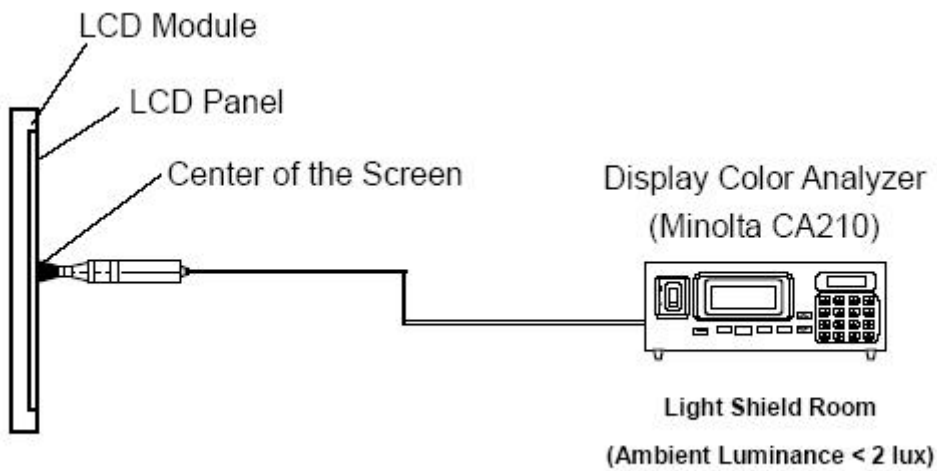
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Measured Response Time	Target																
	0	15	31	47	63	79	95	111	127	143	159	175	191	207	223	239	255
Start																	
0																	
15																	
31																	
47																	
63																	
79																	
95																	
111																	
127																	
143																	
159																	
175																	
191																	
207																	
223																	
239																	
255																	

Note 4: The measure method



(a) : The measurement point is the center of the active area except for the measurement of Luminance Uniformity

(b) : Photometer :CA-210

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5.0 Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50°C , 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50°C , 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0°C , 300hours	
High Temperature Storage (HTS)	Ta= 60°C , 300hours	
Low Temperature Storage (LTS)	Ta= -20°C , 300hours	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: EN61000-4-2, ESD class B: Certain performance degradation allowed

No data lost

Self-recoverable

No hardware failures.

	PRODUCTION SPECIFICATION OF TFT LCD MODULE	Model No: M430BF91 C1
		OC PN: HV430FHB-F91

6.0 Shipping Label

6.1 Panel Label



43寸 BOE 液晶模组
Model No: M430BF91 C1
OC PN : HV430FHB-F91



M430BPR3A112C0221

电流电压 : 61~70V , 700mA,

RoHS

6.2 Carton Label



ABCDEFGHIJKLMN

Model No:(型号): M430BF91 C1

OC PN : HV430FHB-F91

电流电压: 61-70V 600mA/720mA

QTY(数量) : 4 PCS/CTN

N.W(净重) : KG

G.W(毛重) : KG



	PRODUCTION SPECIFICATION OF TFT LCD MODULE	Model No: M430BF91 C1
		OC PN: HV430FHB-F91

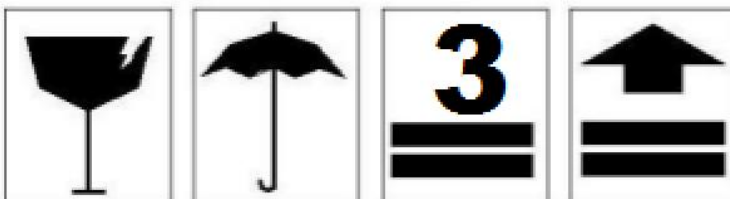
7. Packaging

9.1 Carton(internal package)

- (1)Packaging Form
- (2) Packaging Method
- (3) Carton box size :
- (4) Gloss weight of 1 carton:
- (5) Packing pictures :

Note 1) Acceptable number of piling : 4 sets

7.2 Packing Mark



	PRODUCTION SPECIFICATION OF TFT LCD MODULE	Model No: M430BF91 C1
		OC PN: HV430FHB-F91

8. PRECAUTION

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- 1 Do not apply rough force such as bending or twisting to the module during assembly.
- 2 To assemble or install module into user's system can be in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- 3 It's not permitted to have pressure or impulse on the module because the LED panel and Backlight will be damaged.
- 4 Always follow the correct power sequence when LED module is connecting and operating. This can prevent damage to the CMOS LSI chips during latch-up.
- 5 Do not pull the I/F connector in or out while the module is operating .
- 6 Do not disassemble the module.
Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very
- 7 soft and easily scratched.
- 8 It is dangerous that moisture come into or contacted the LED module, because moisture may damage LED module when it is operating.
- 9 High temperature or humidity may reduce the performance of module. Please store LED module within the specified storage conditions.
- 10 When ambient temperature is lower than 10 °C may reduce the display quality. For example, the response time will become slowly.

8.2 SAFETY PRECAUTIONS

- 1 It is dangerous that moisture come into or contacted the LED module, because the moisture may damage LED module when it is operating.
- 2 If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth, in case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- 3 After the module's end of life, it is not harmful in case of normal operation and storage.

	PRODUCTION SPECIFICATION OF TFT LCD MODULE	Model No: M430BF91 C1
		OC PN: HV430FHB-F91

9. Outline dimensions

